

Fig. 1 (Prior Art)

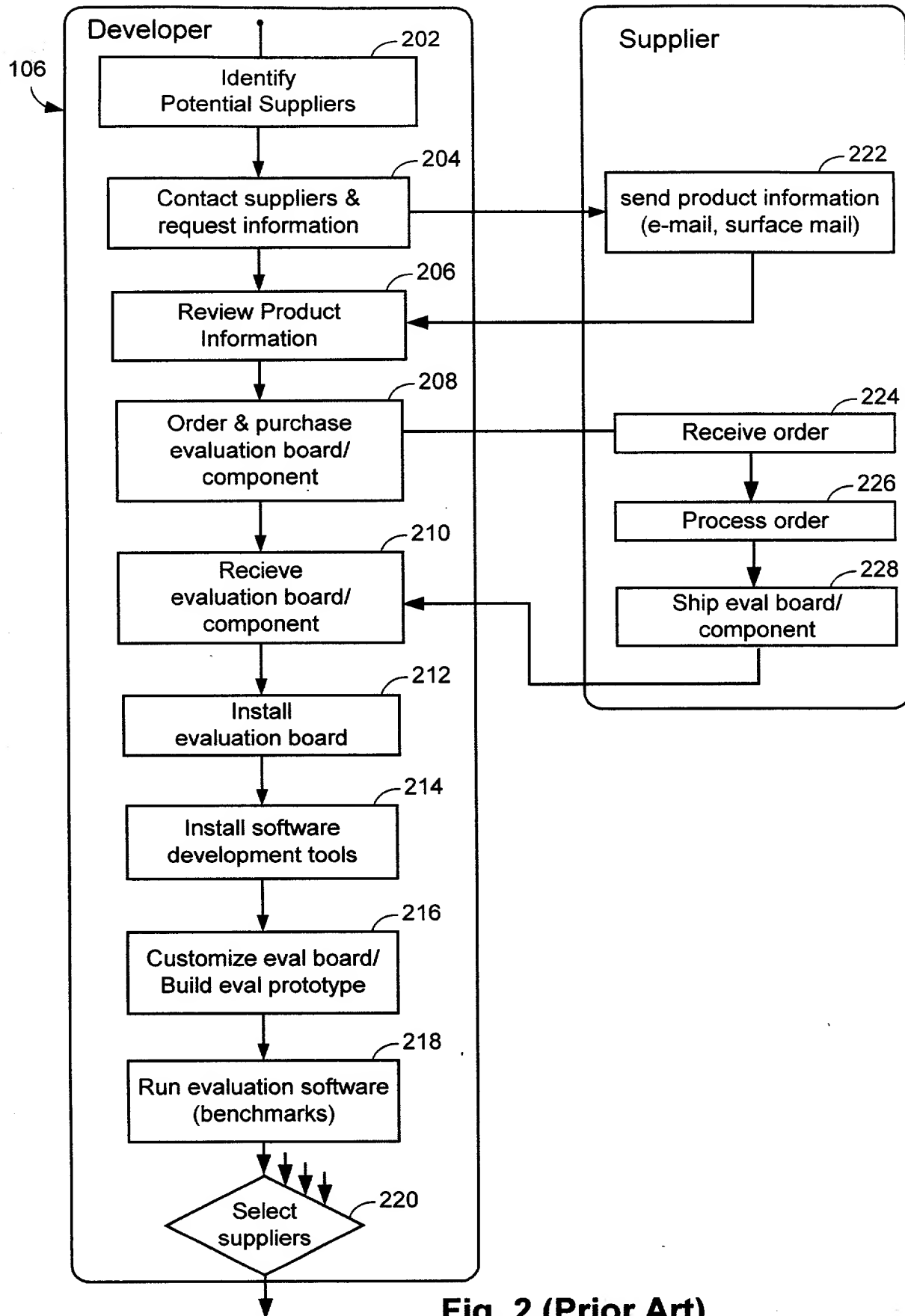


Fig. 2 (Prior Art)



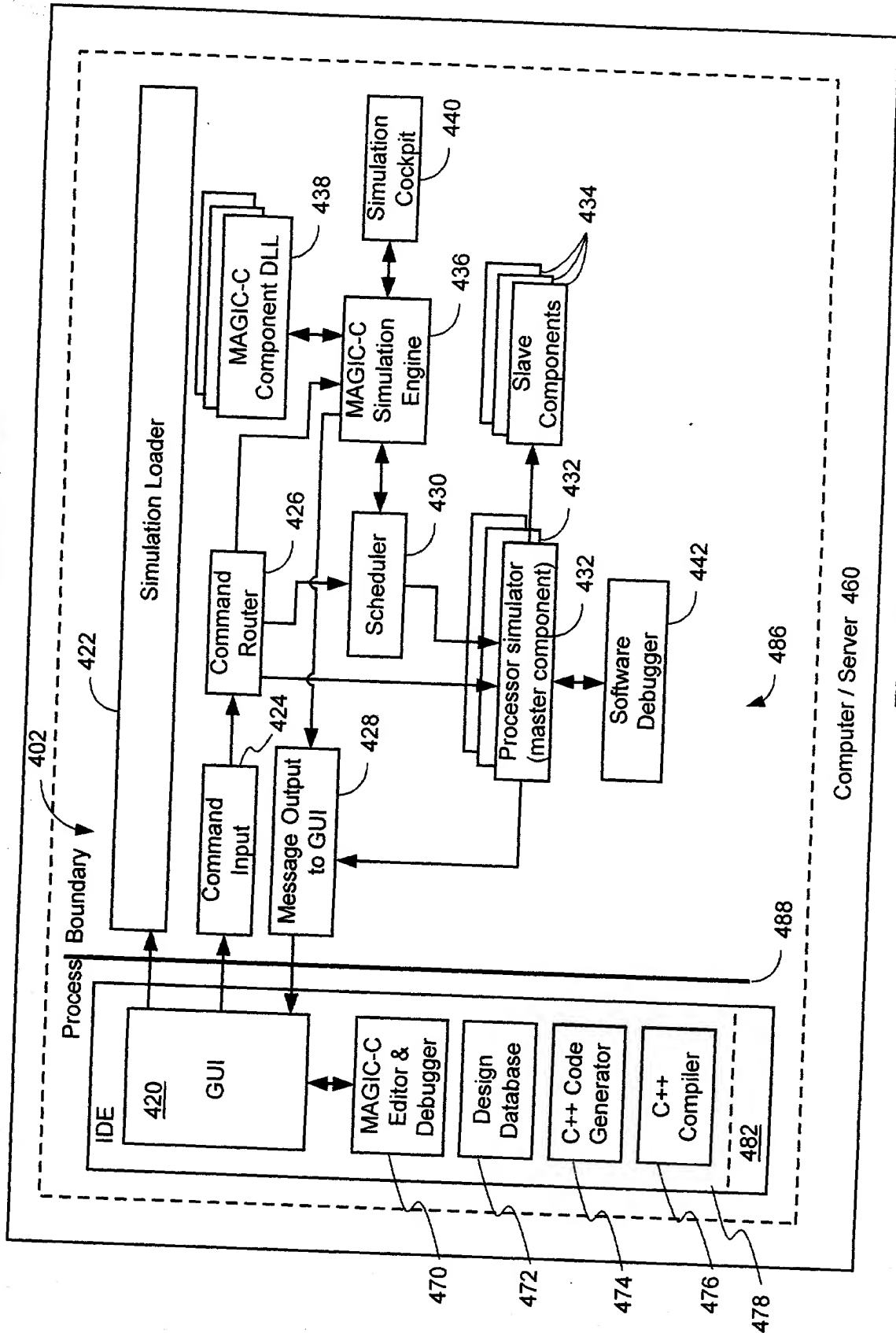


Fig. 4A

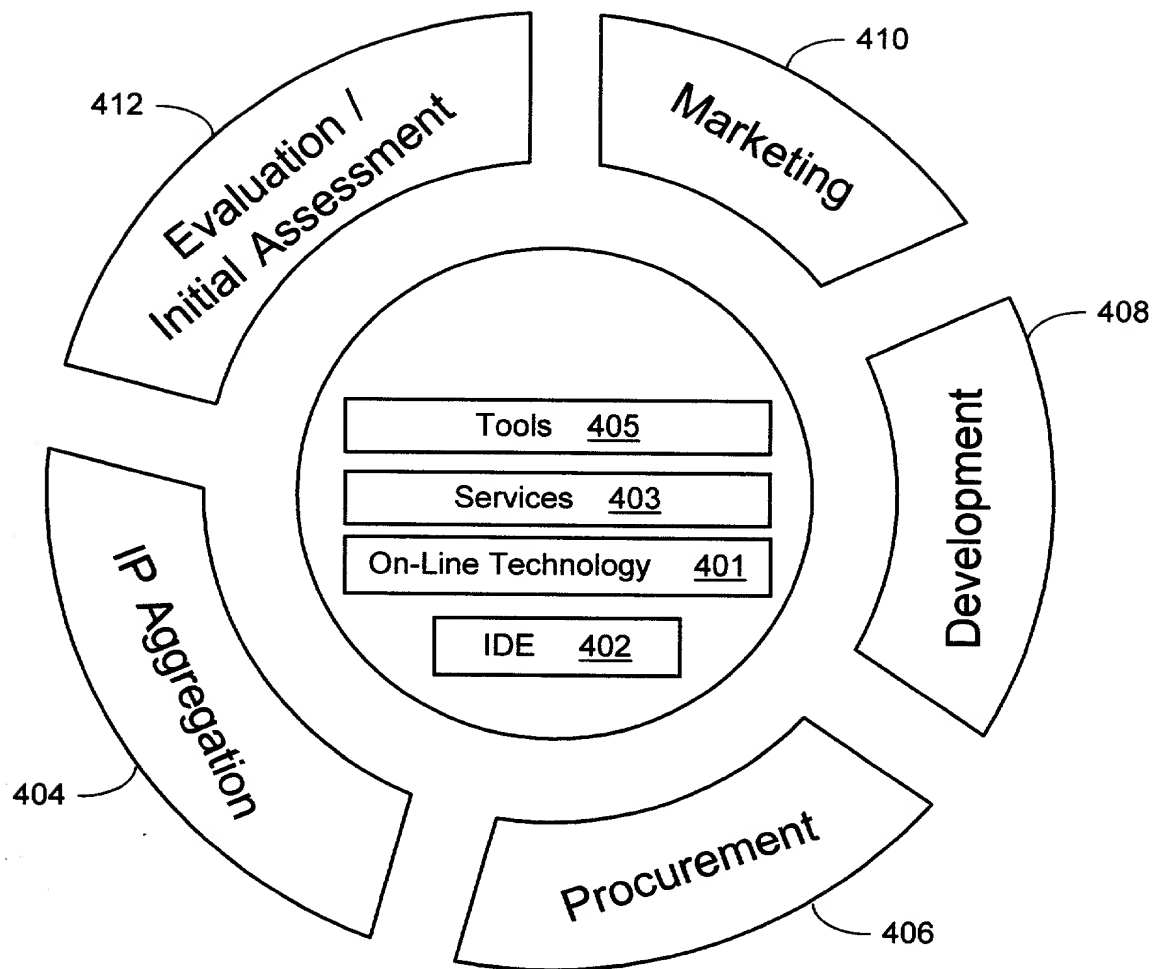


Fig. 4B

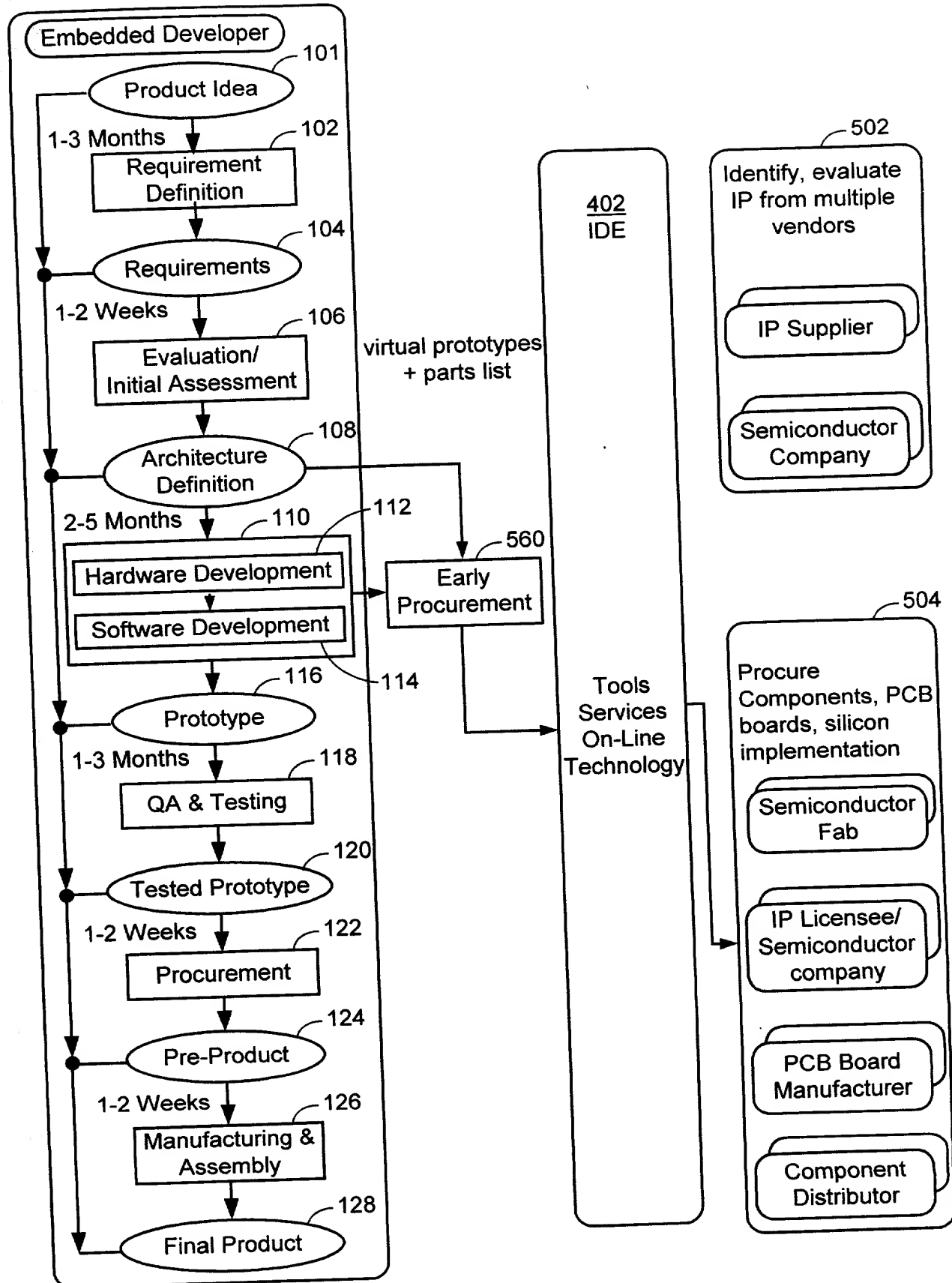


Fig. 5

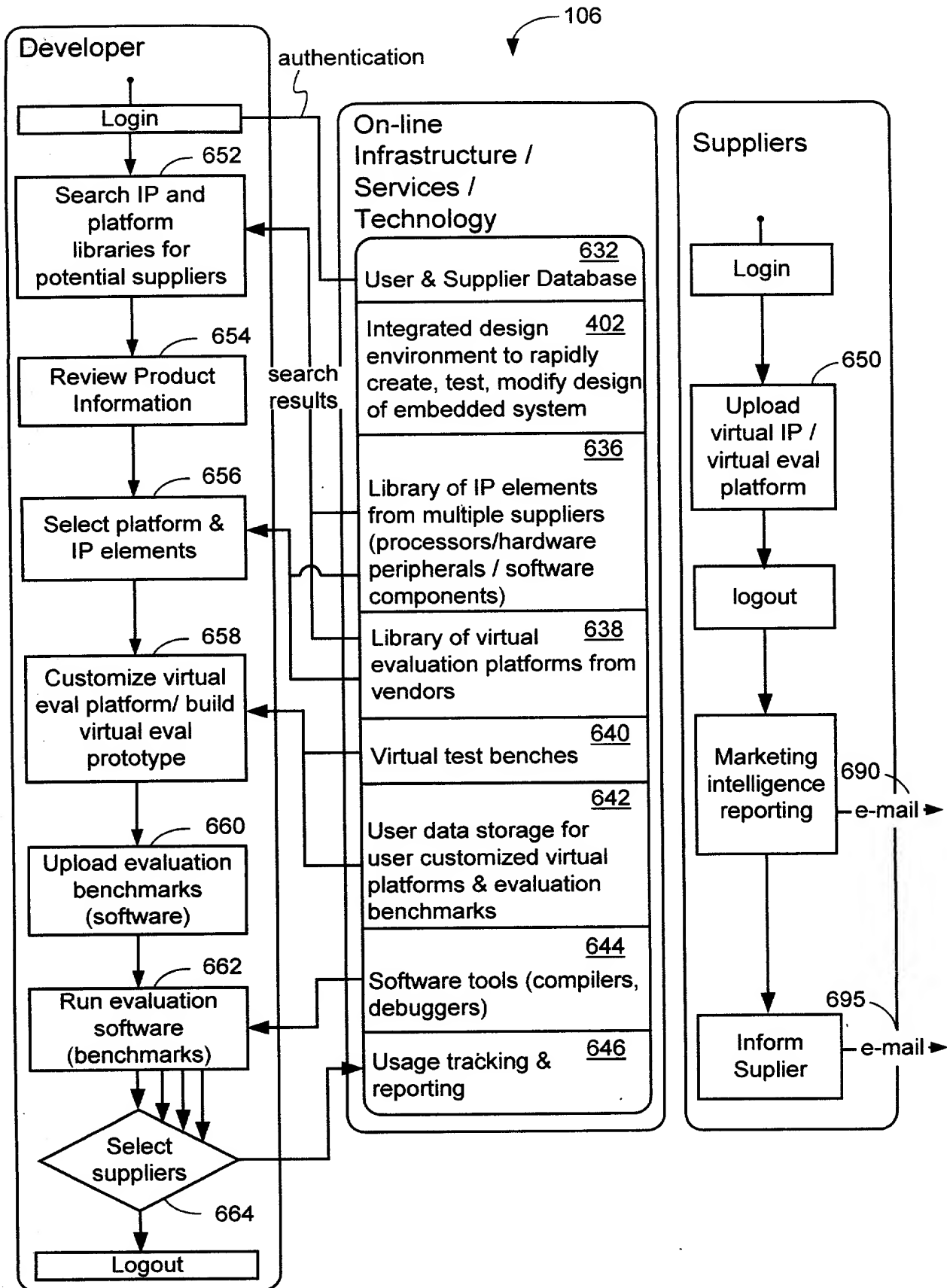


Fig. 6

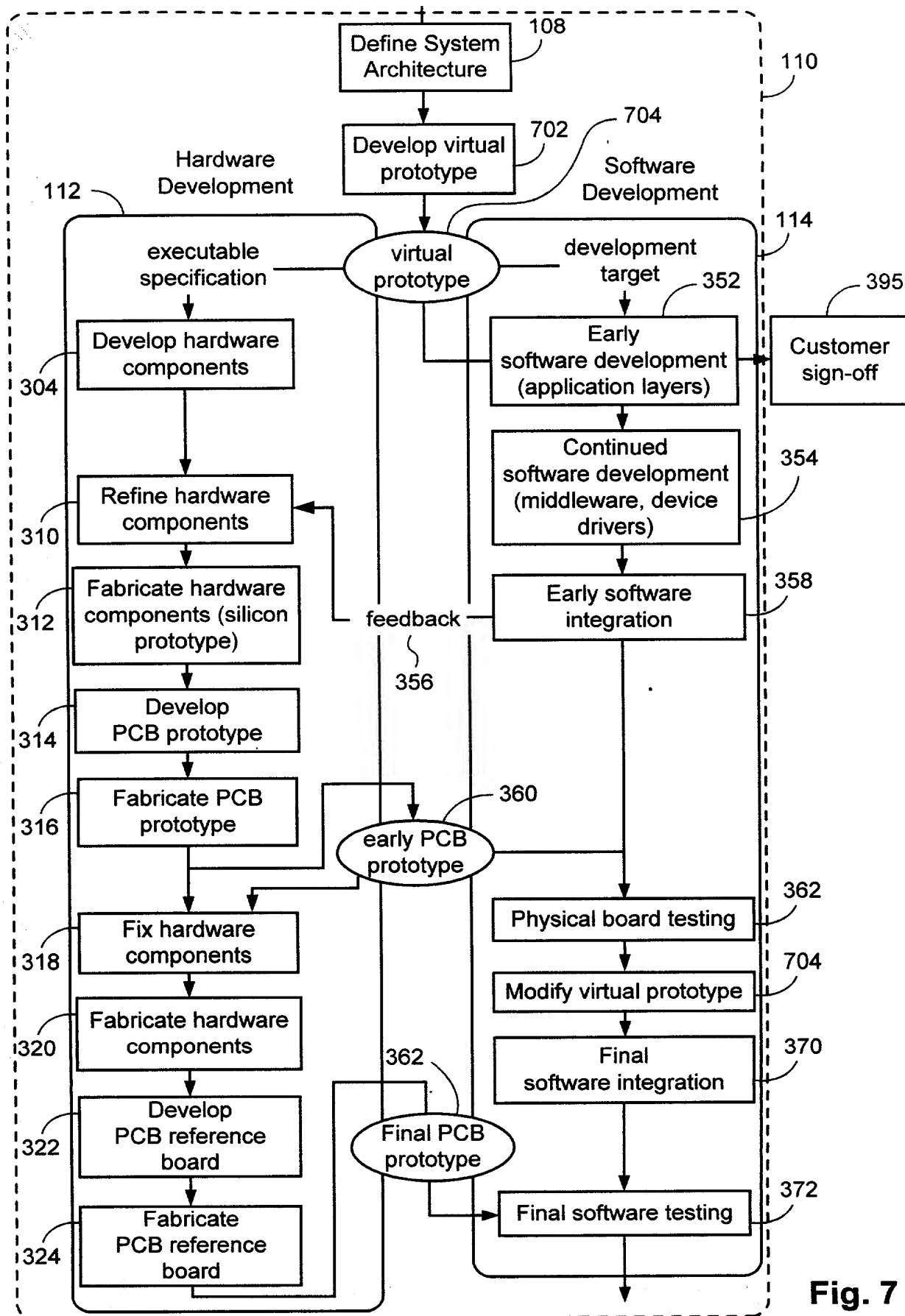


Fig. 7

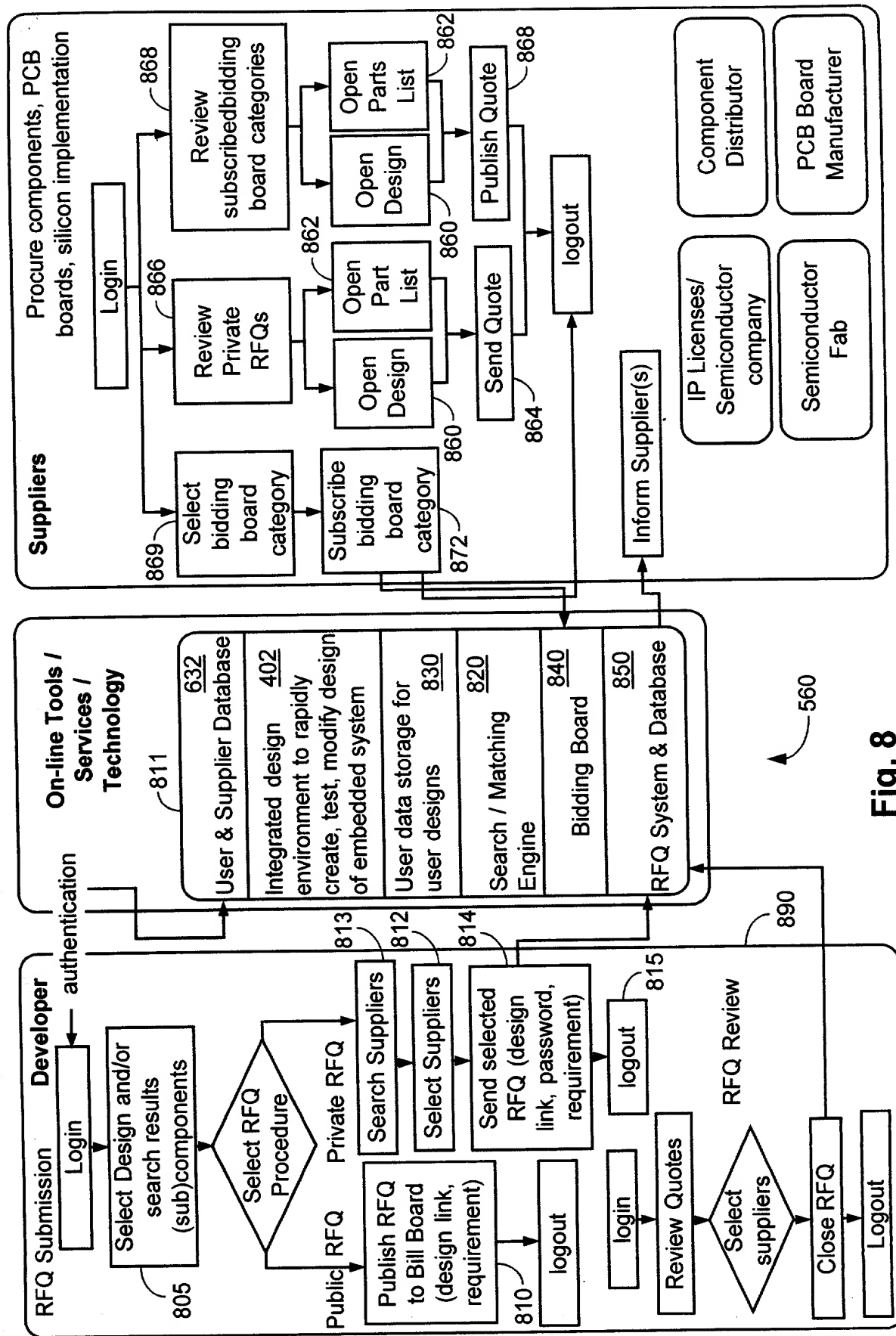


Fig. 8

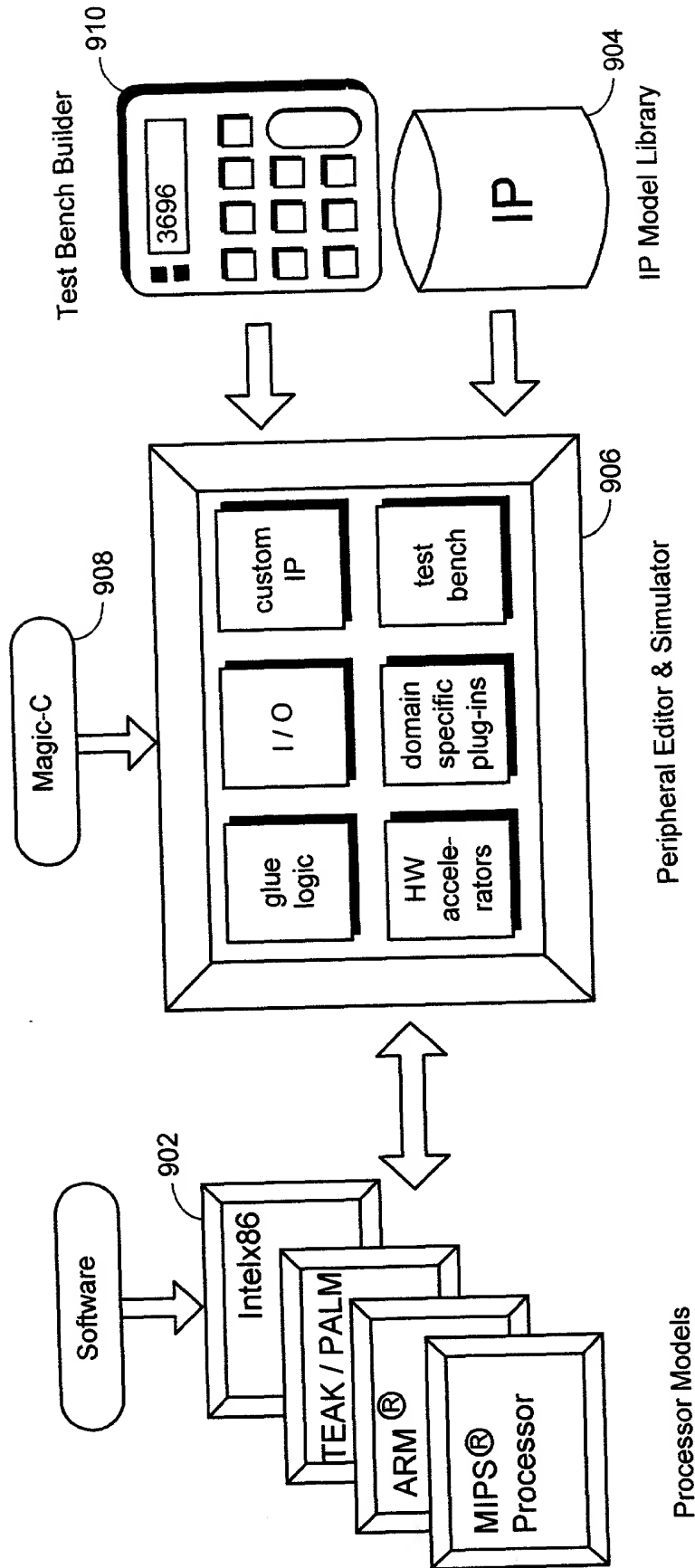


Fig. 9

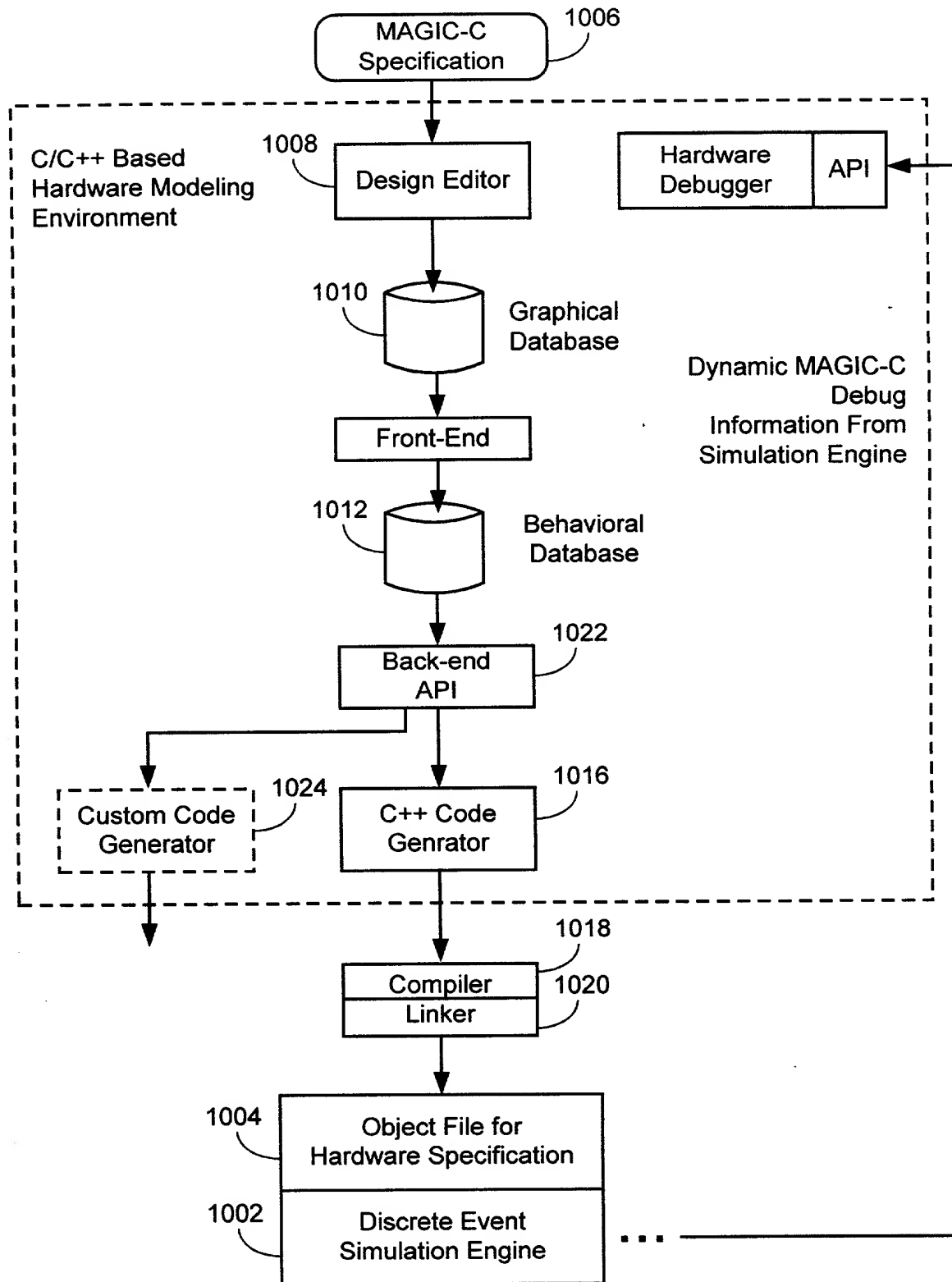


Fig. 10

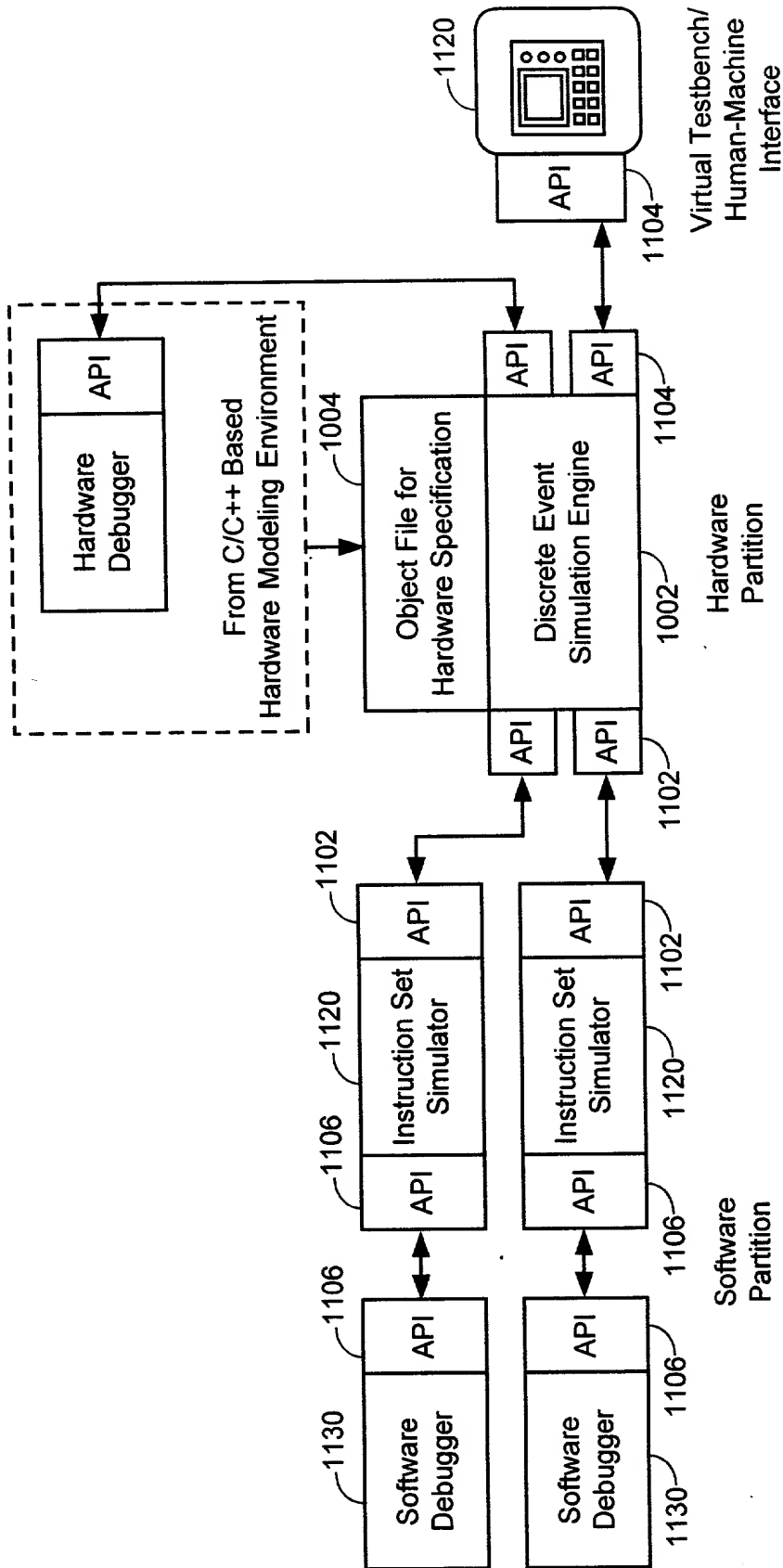


Fig. 11

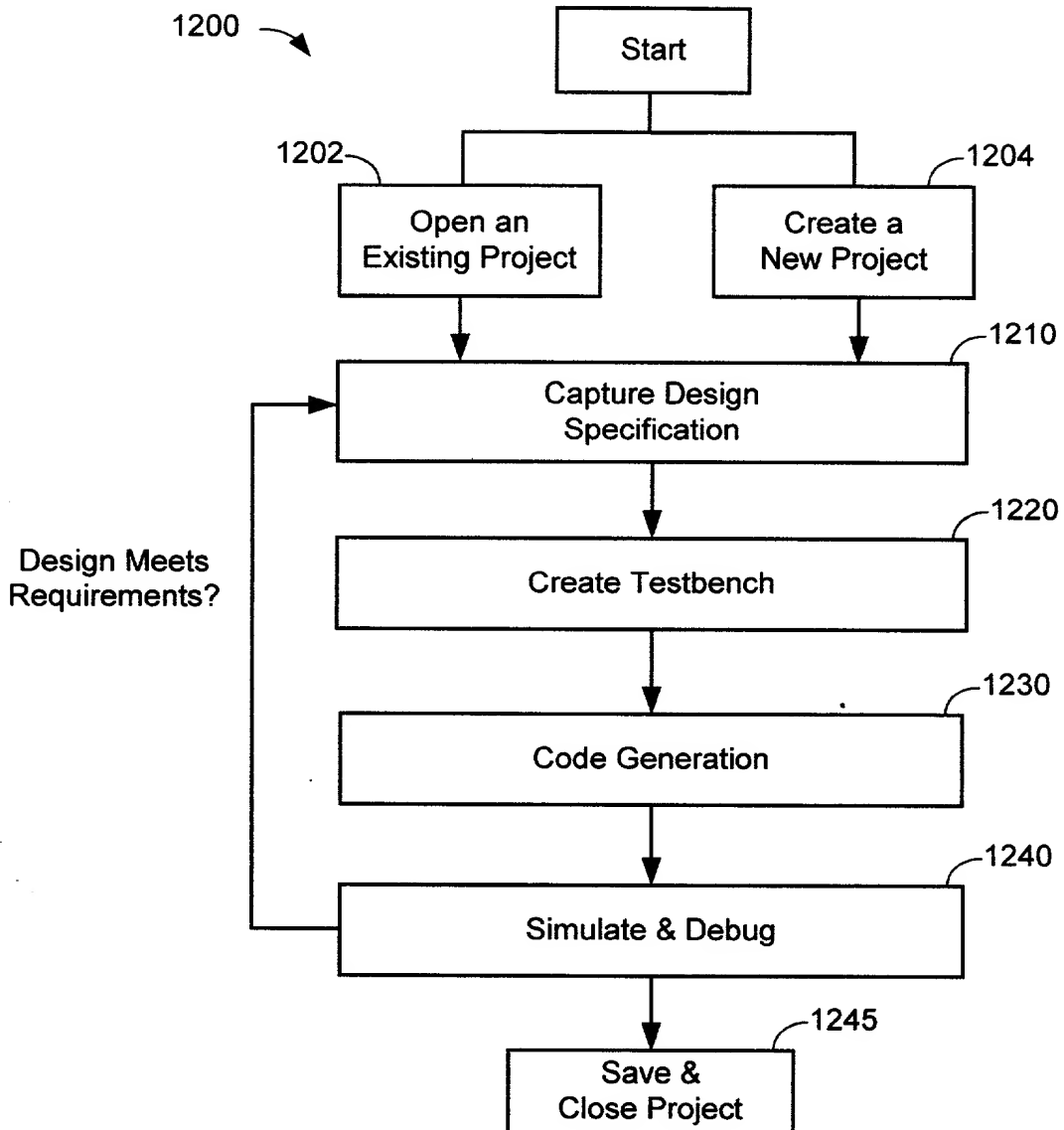


Fig. 12

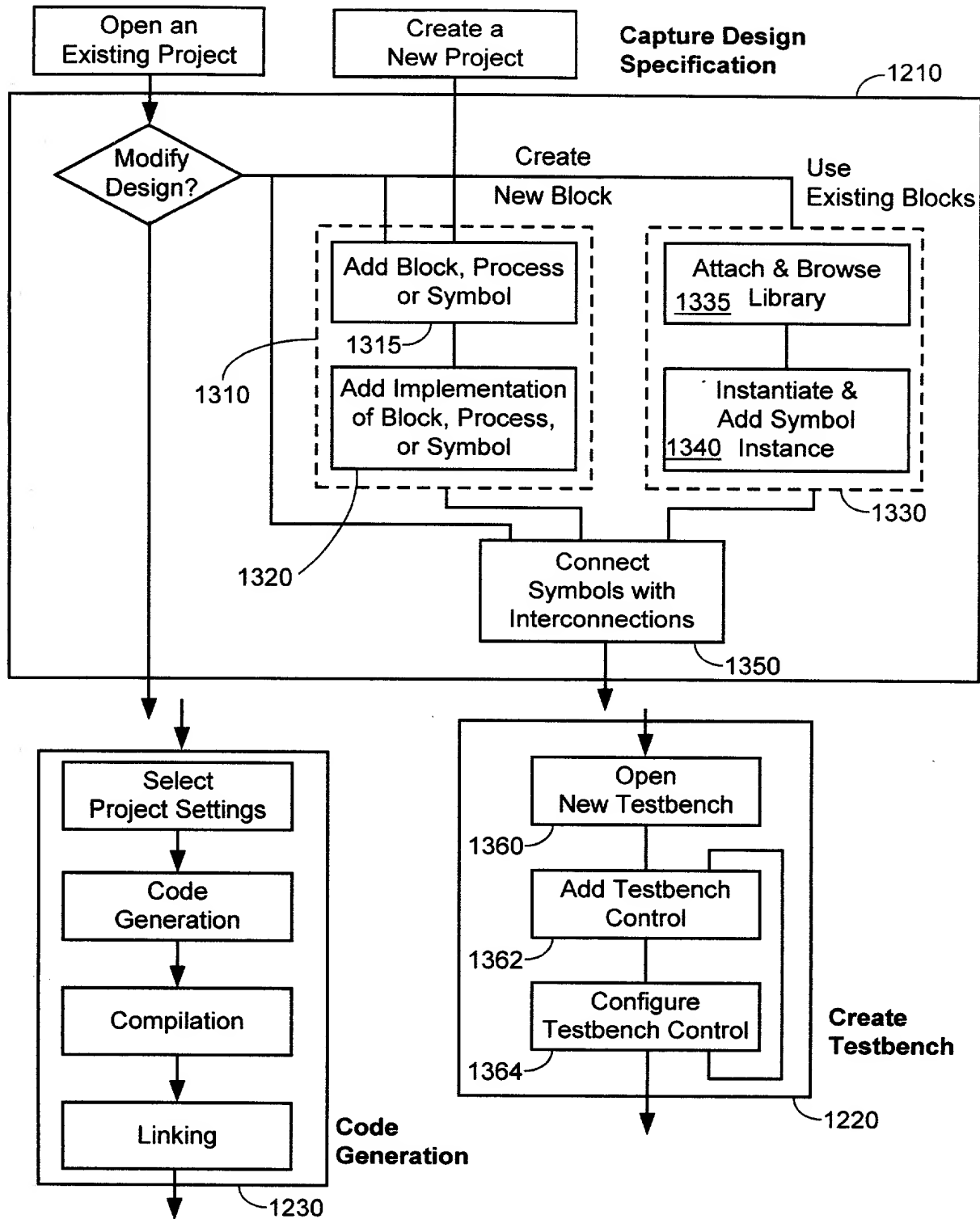


Fig. 13

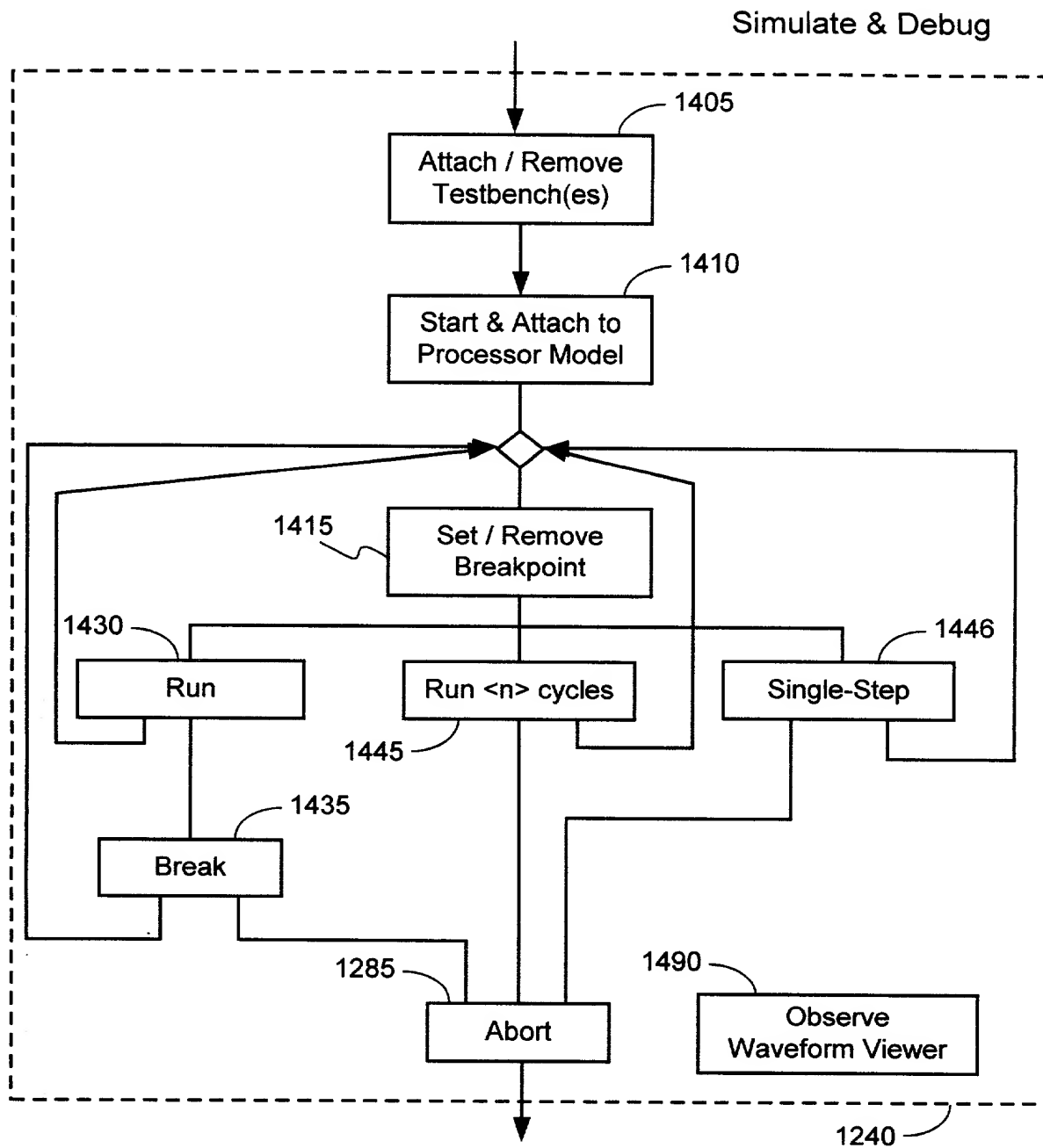


Fig. 14

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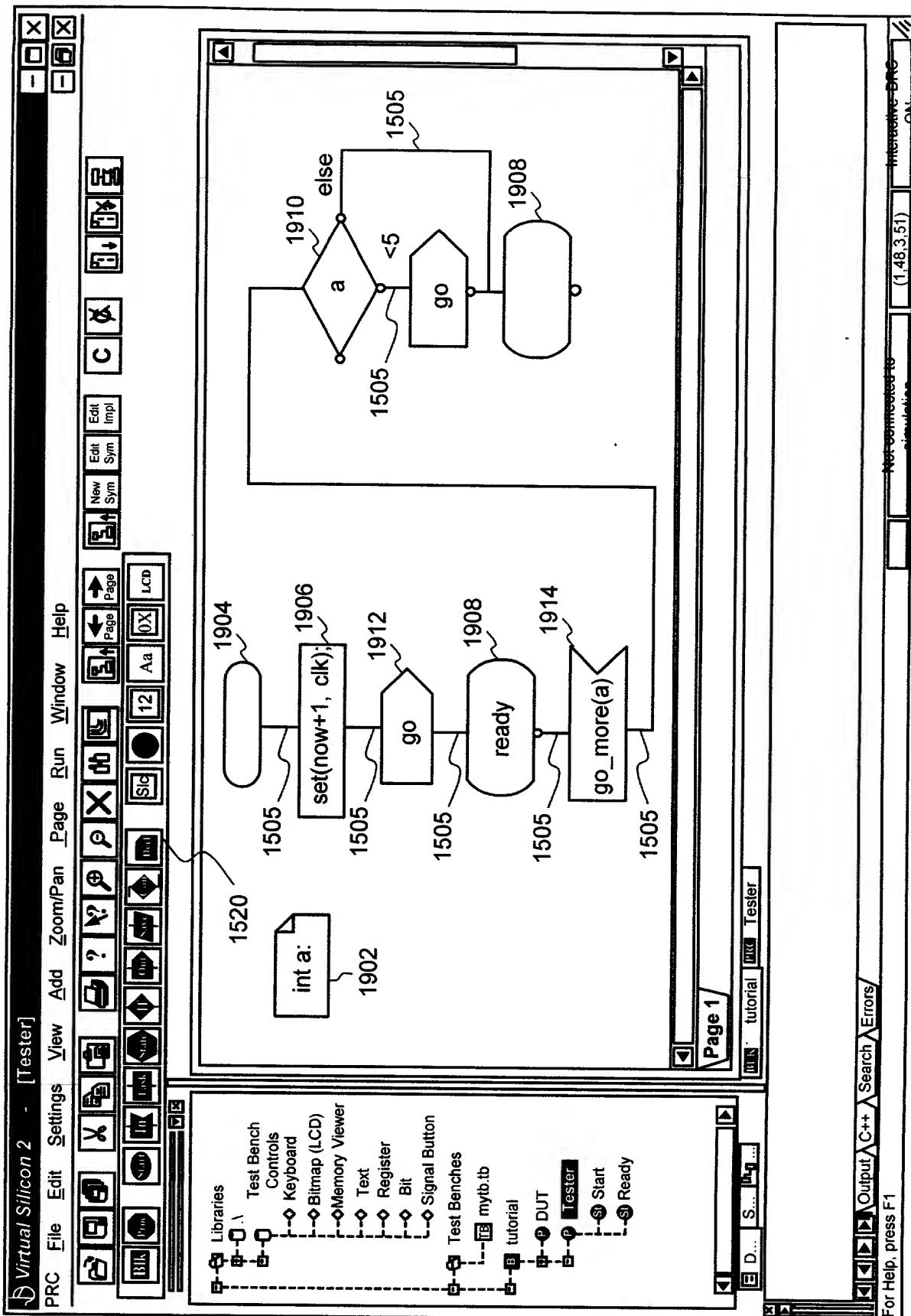


Fig. 15

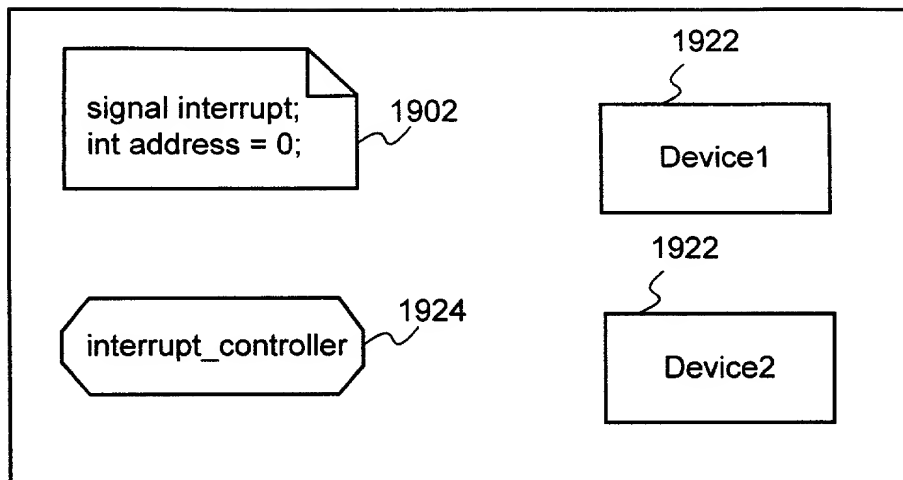


Fig. 16

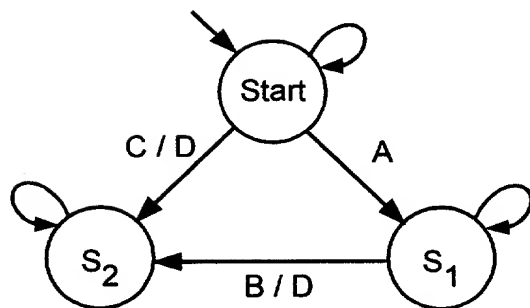


Fig. 17(a)

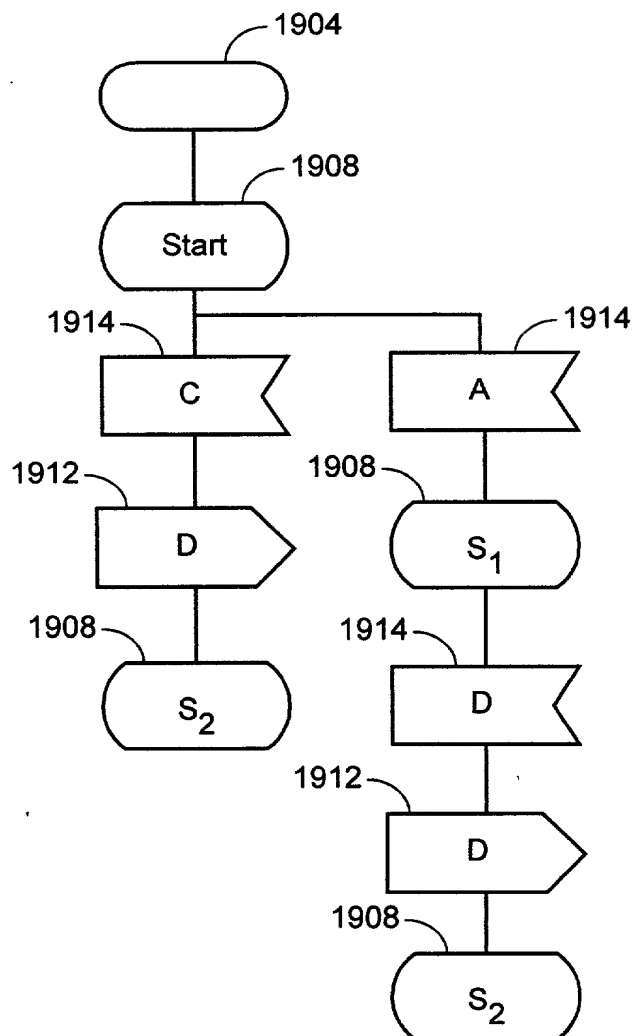


Fig. 17(b)

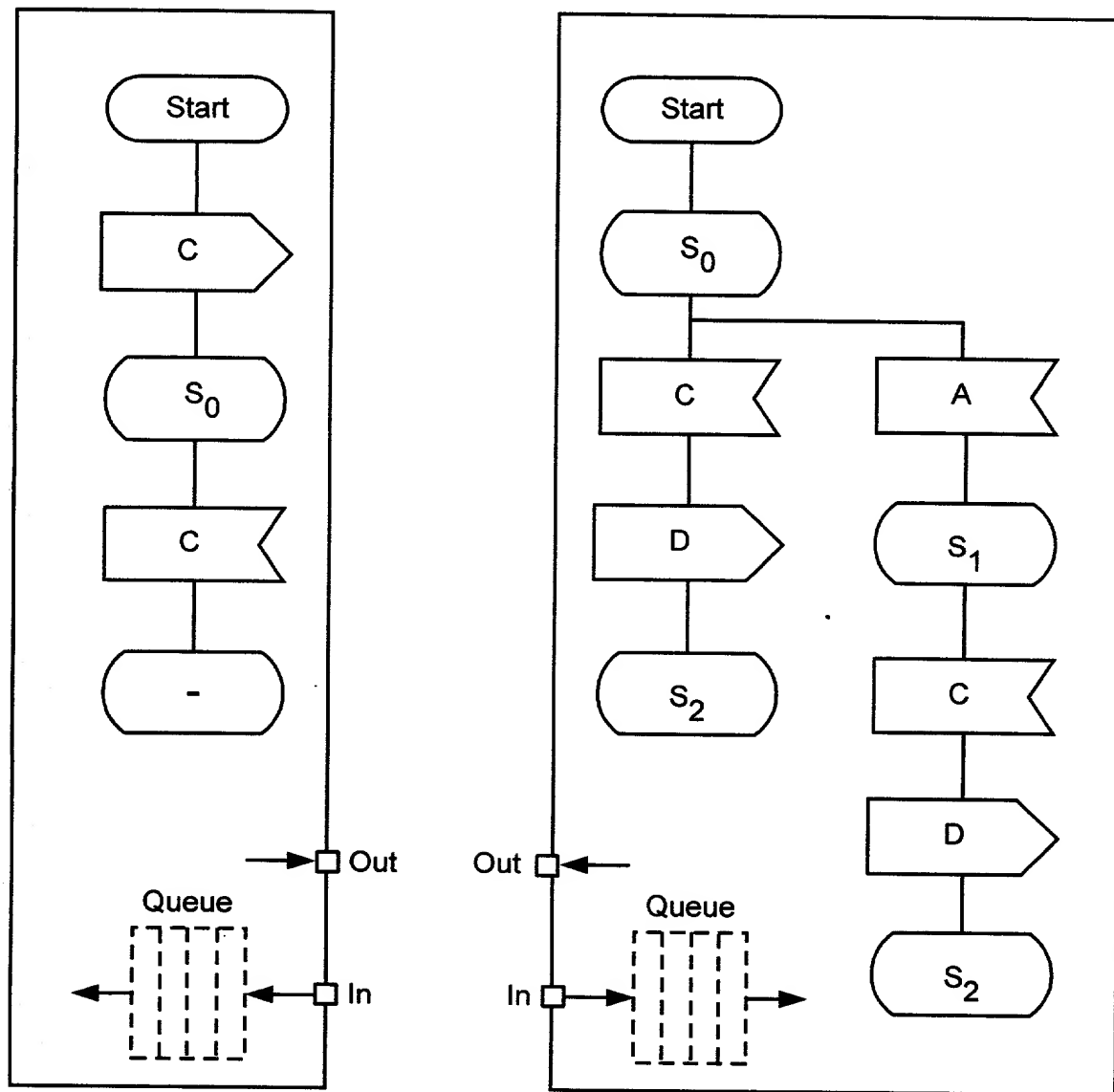


Fig. 18

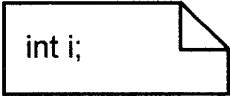

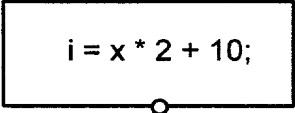
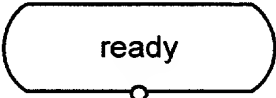
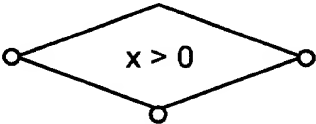
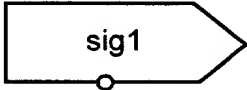
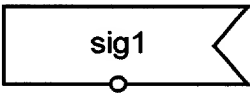
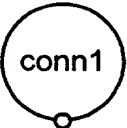
	Name	Graphical Symbol	Description
1902	Declaration		defines local variables and signals.
1904	Start		Starting point of the Finite State Machine execution at initialization time
1906	Task		Execution block, containing ANSI-C statements to be executed
1908	State		Location where FSM waits in until a triggering signal is received.
1910	Decision		Directs execution flow based on the result of expression evaluation inside the decision construct.
1912	Signal-Out		Sending of a communication signal (with an optional payload)
1914	Signal-In		Receiving of a communication signal (with an optional payload)
1916	Connector		Allows to split designs over multiple pages, and connects the control flow between these different pages.

Fig. 19A

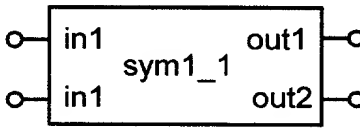


1920	Symbol		Captures design hierarchy and structure. Communication is done through pins on the outline of the symbol. Allows to re-use functional behavior by supporting multiple instances
1922	Blocks		Captures design hierarchy and structure. Communication is done through signals declared at higher scopes. Communication is done by signal name matching (rather than pin connection). A block can contain multiple processes.
1924	Process		Acts as leaf node in the design hierarchy, and captures a single FSM. By definition, all processes are concurrent at all times.

Fig. 19B

```
// External interface
extern_signal WR(unsigned int, unsigned int,
unsigned int);
extern_signal RD(unsigned int, unsigned int);
extern_signal Write_Ack;
extern_signal Read_Data(unsigned int);
extern_signal CNTINTR(unsigned int);
// Local variables
signal start_clk;
clock clk;
bool clock_started;
unsigned int LIMIT; //write register
VS_int COUNT;
//temp vars
unsigned int data, width, addr;
```

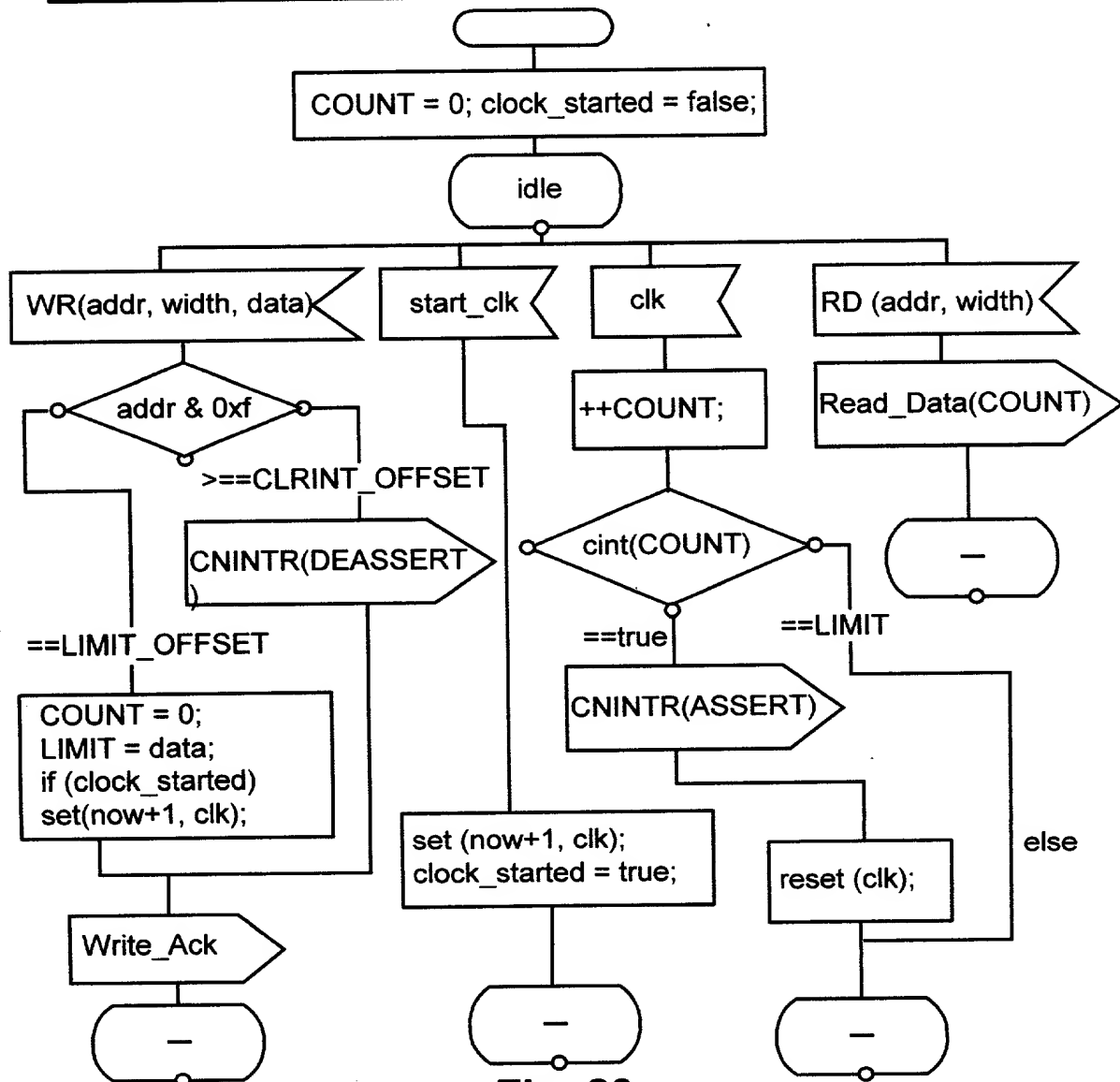


Fig. 20

Design
Window

Test Bench
Builder Toolbar

WaveViewer

Navigation
Toolbar

Symbol Editor
Toolbar

Compiler/Debugger
Toolbar

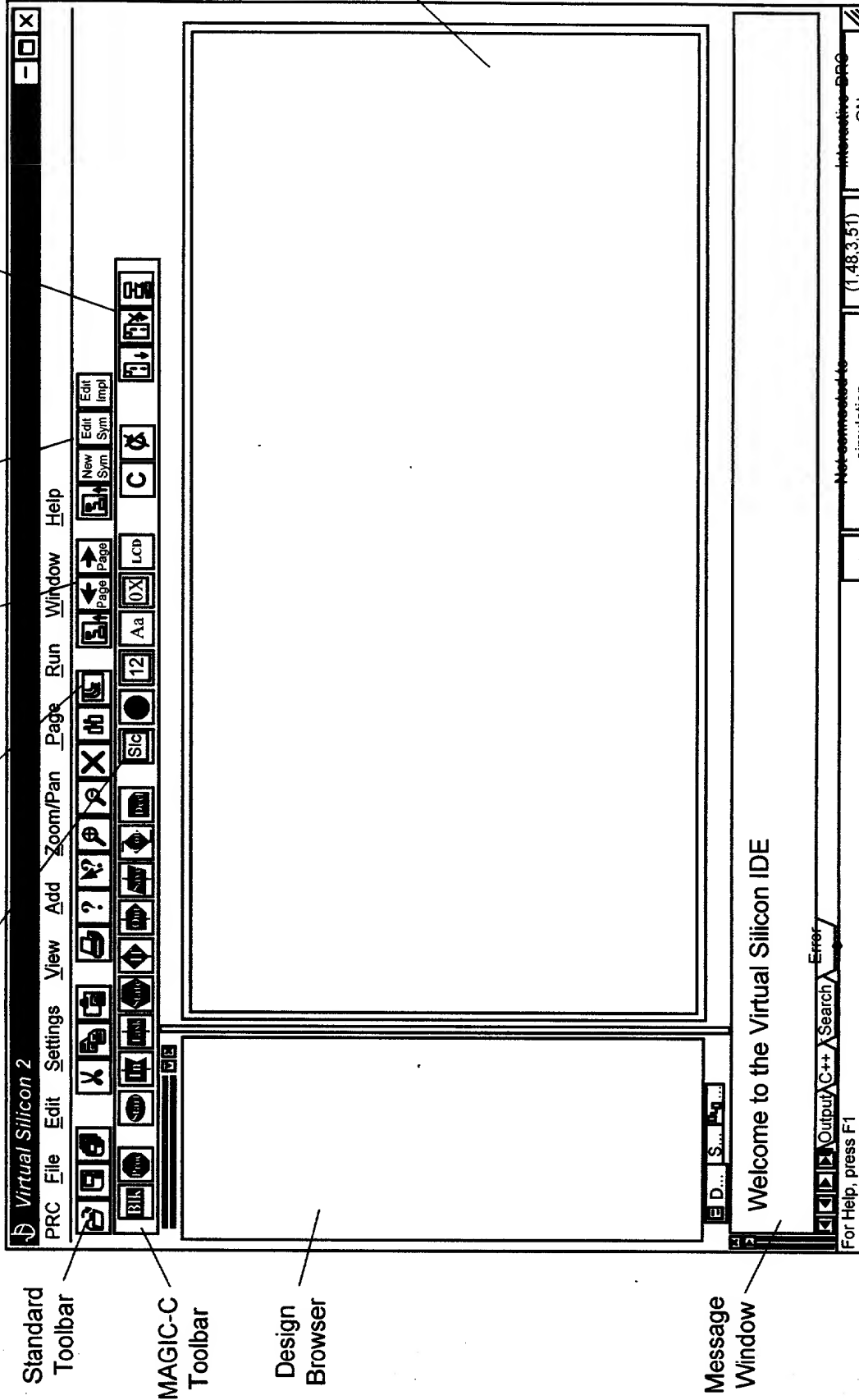
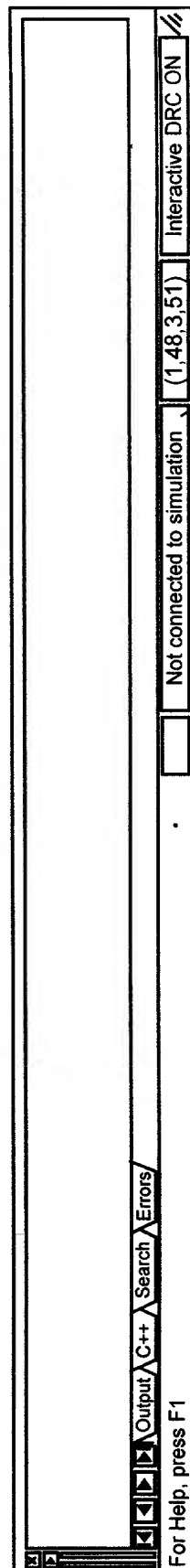


Fig. 21



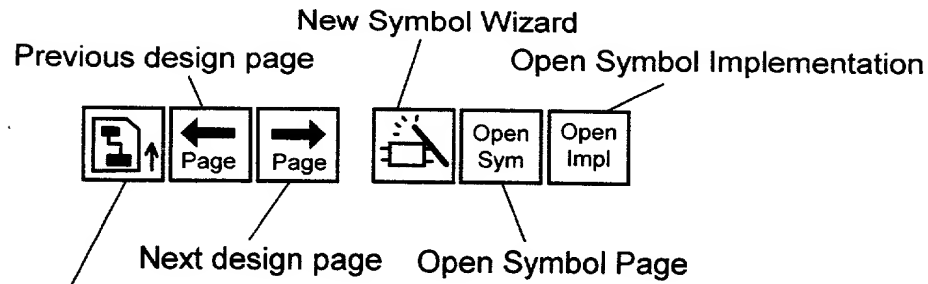
Standard Toolbar

Fig. 22



Message Window, Showing Different Message Tabs, and the Status Bar

Fig. 27



Move up one level (in hierarchy)

Fig. 23

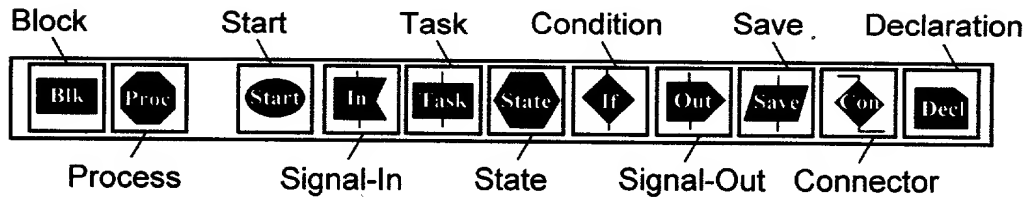


Fig. 24

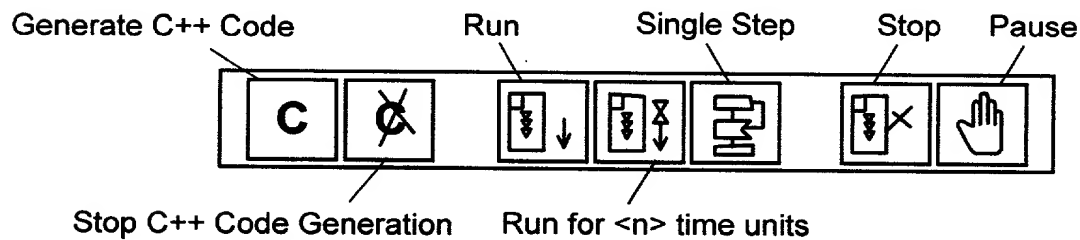


Fig. 25

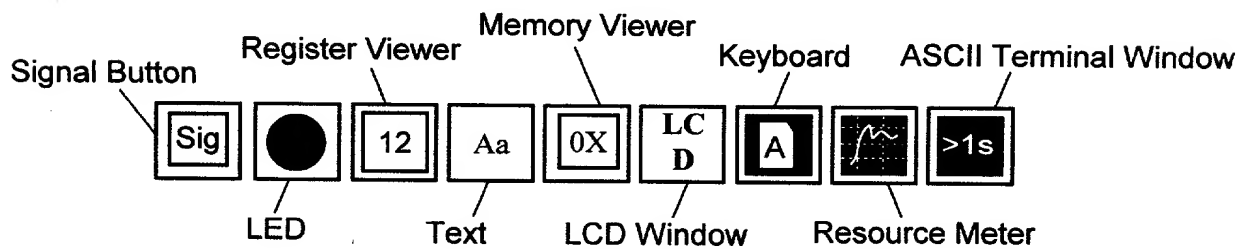


Fig. 26

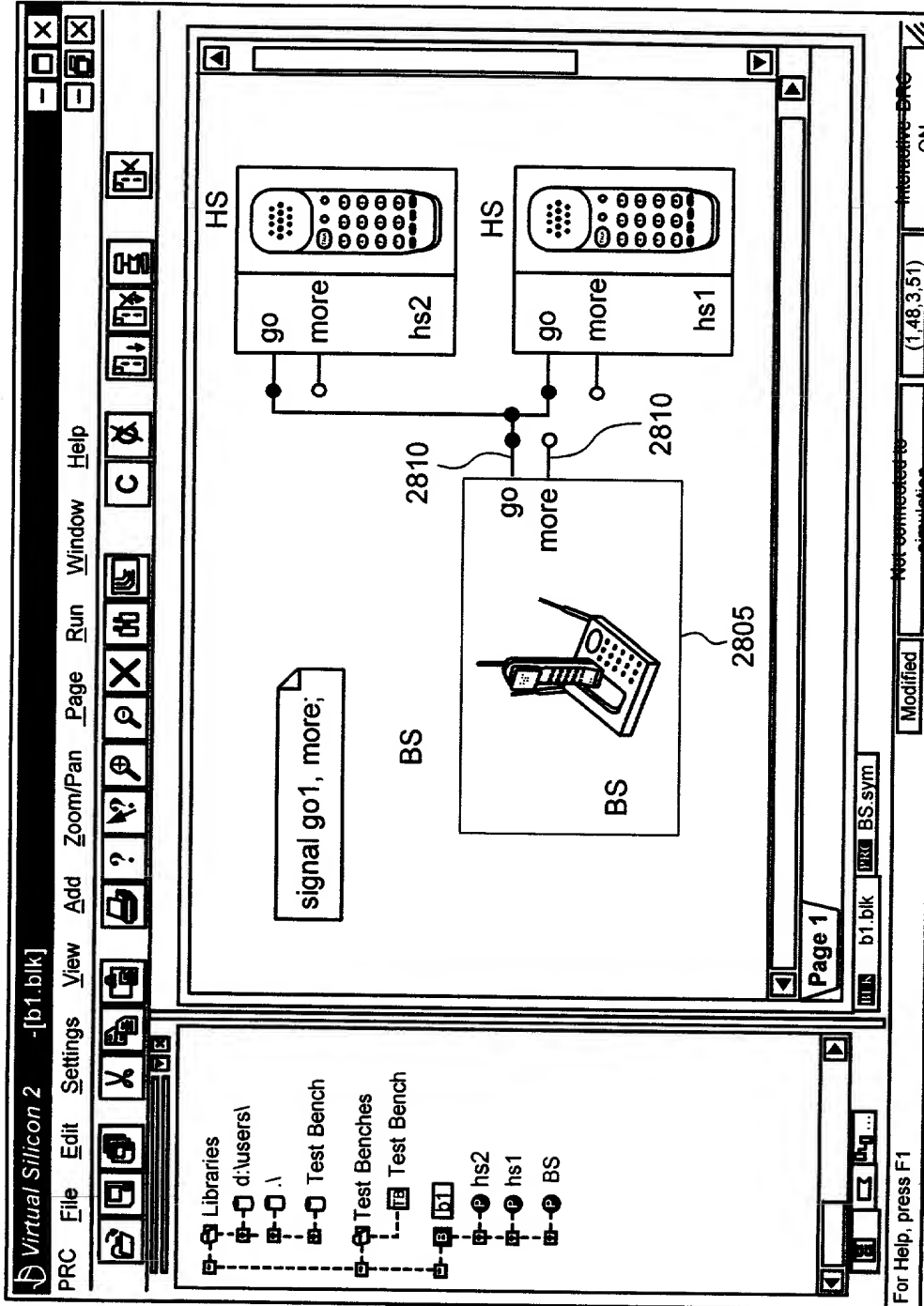


Fig. 28

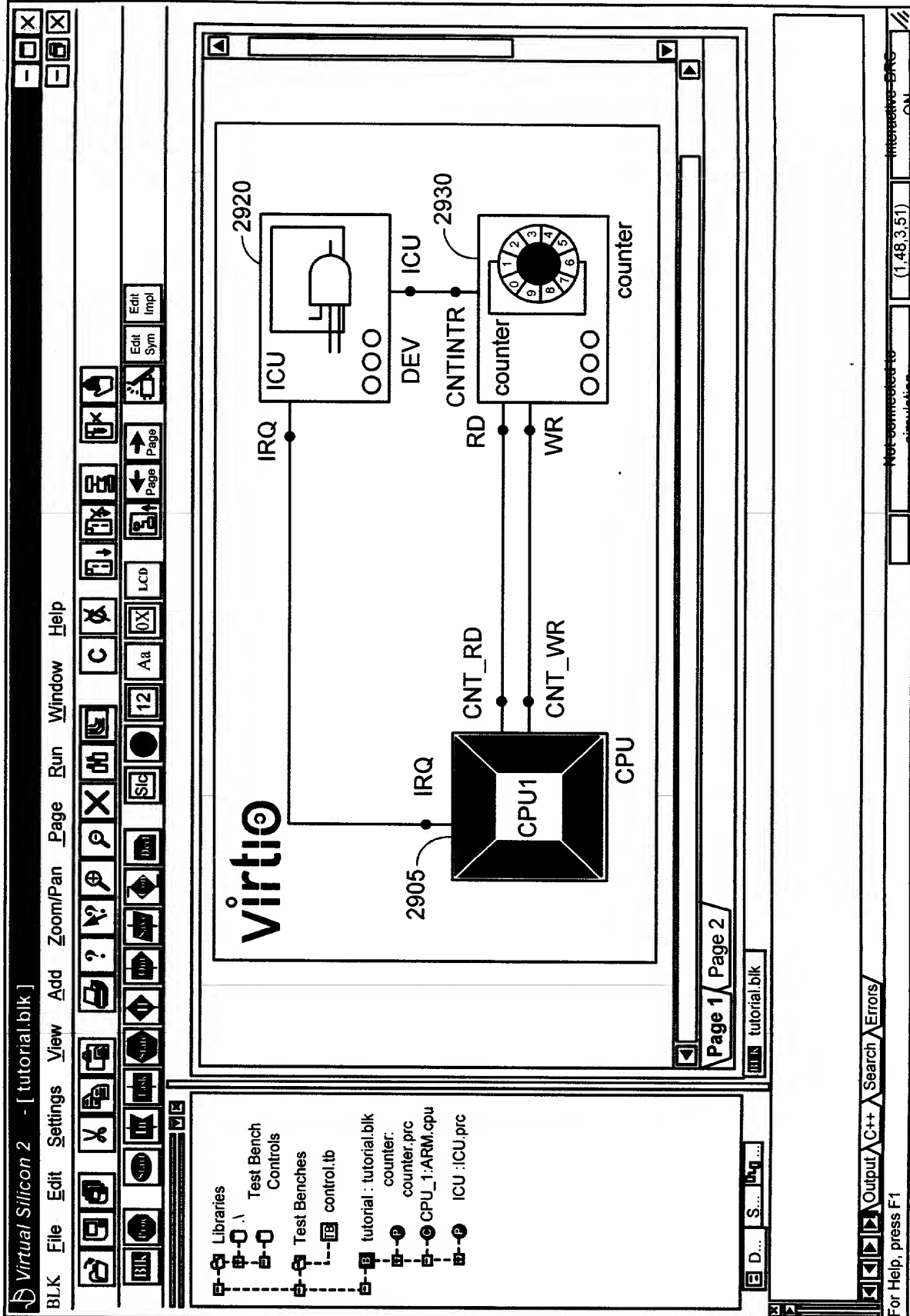


Fig. 29

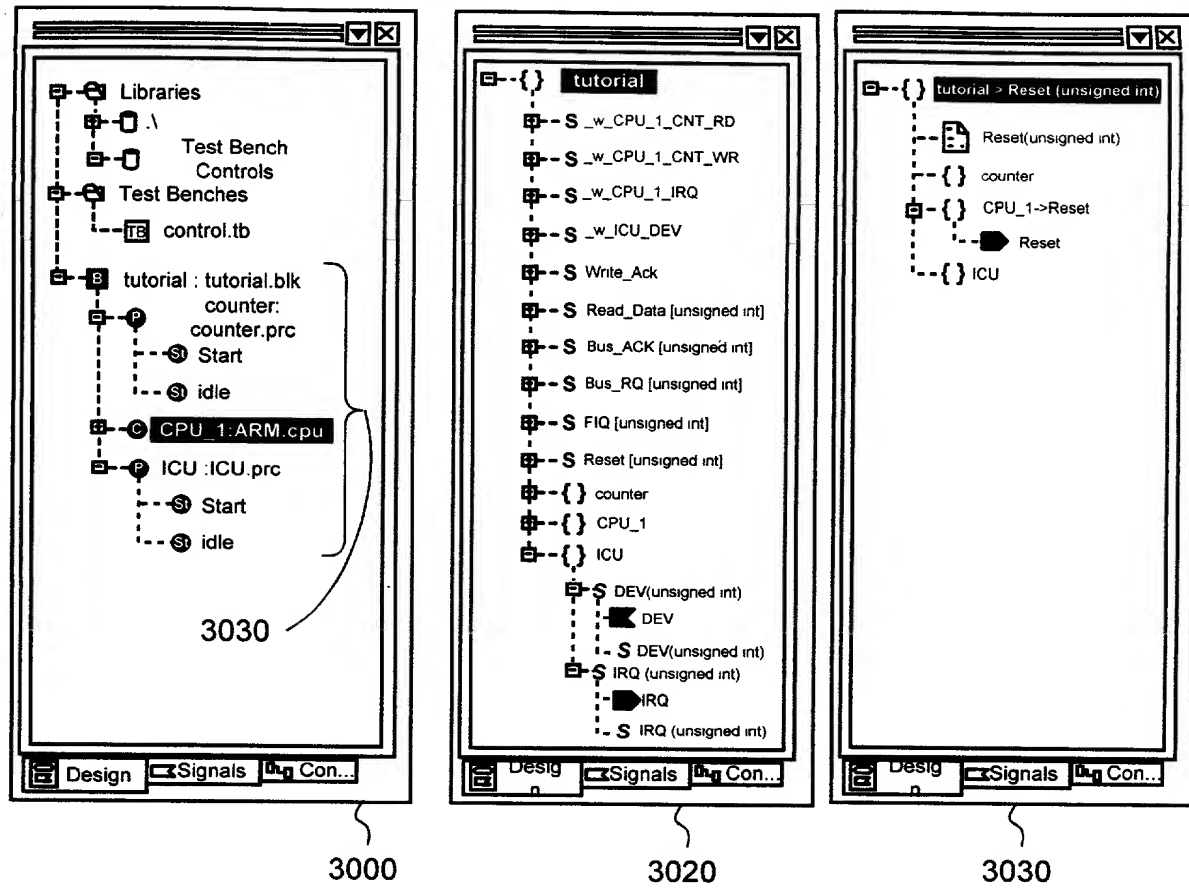


Fig. 30

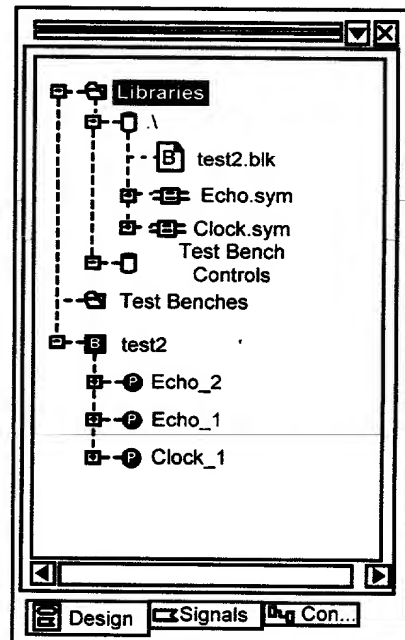


Fig. 31

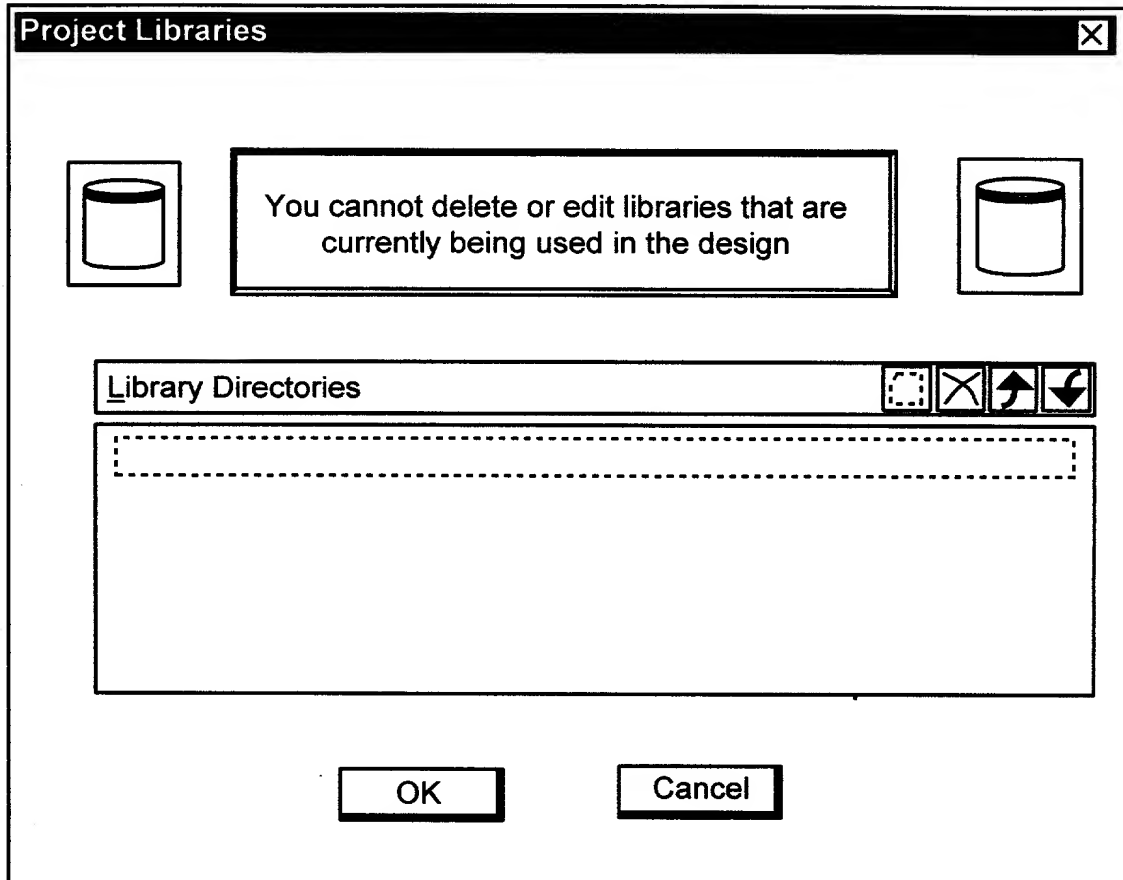
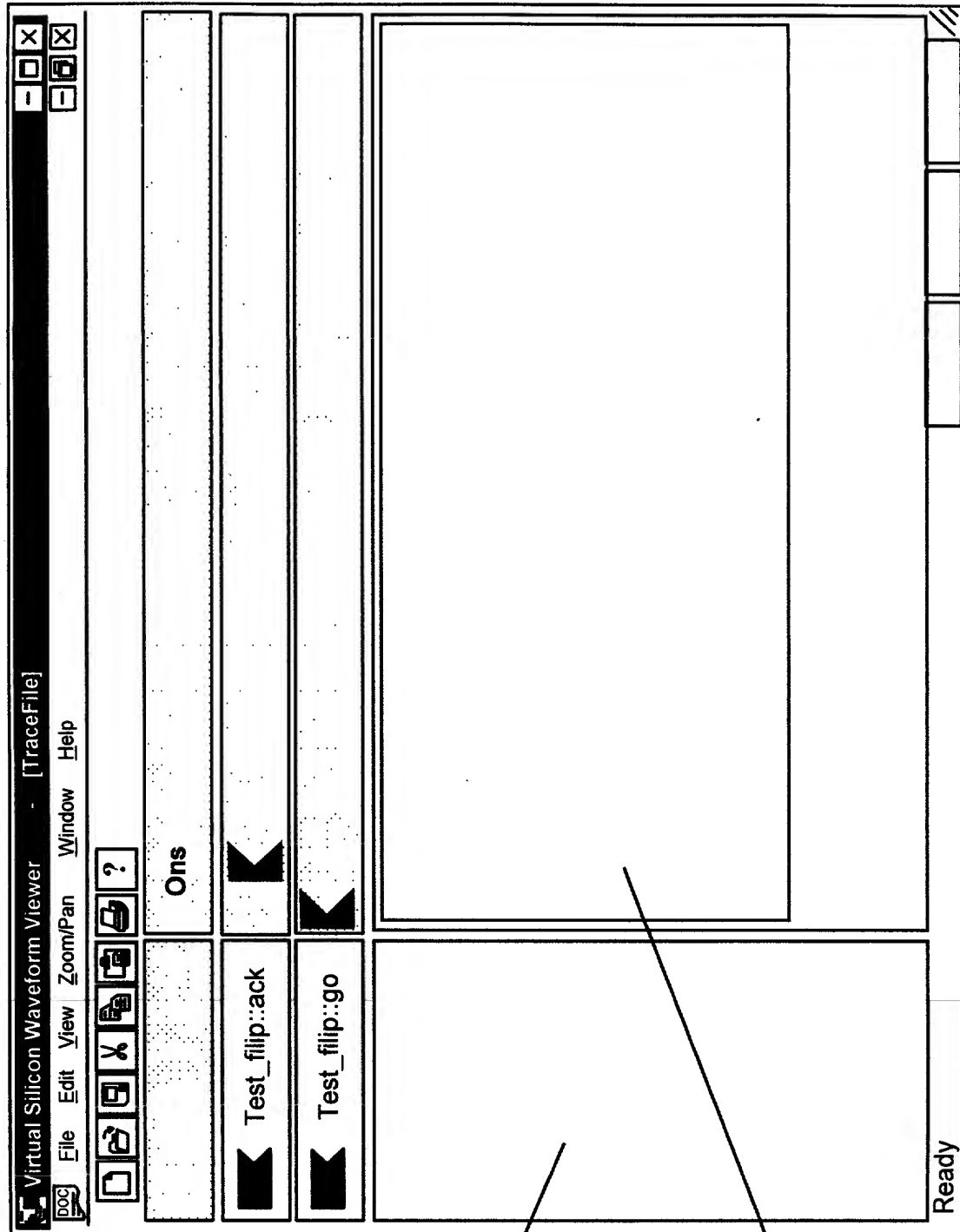


Fig. 32



Name Display
Window

Waveform
Display

Fig. 33A

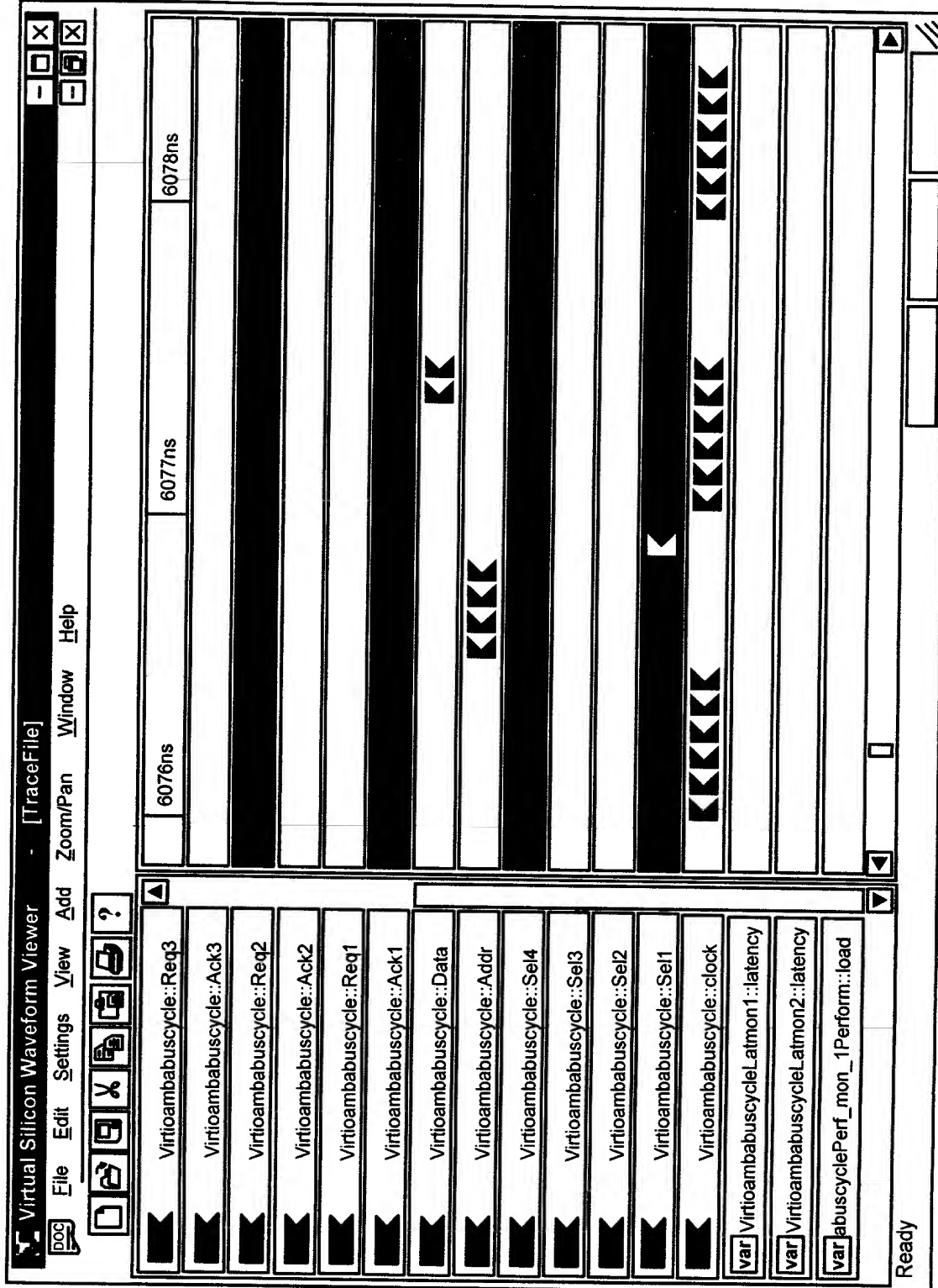


Fig. 33B

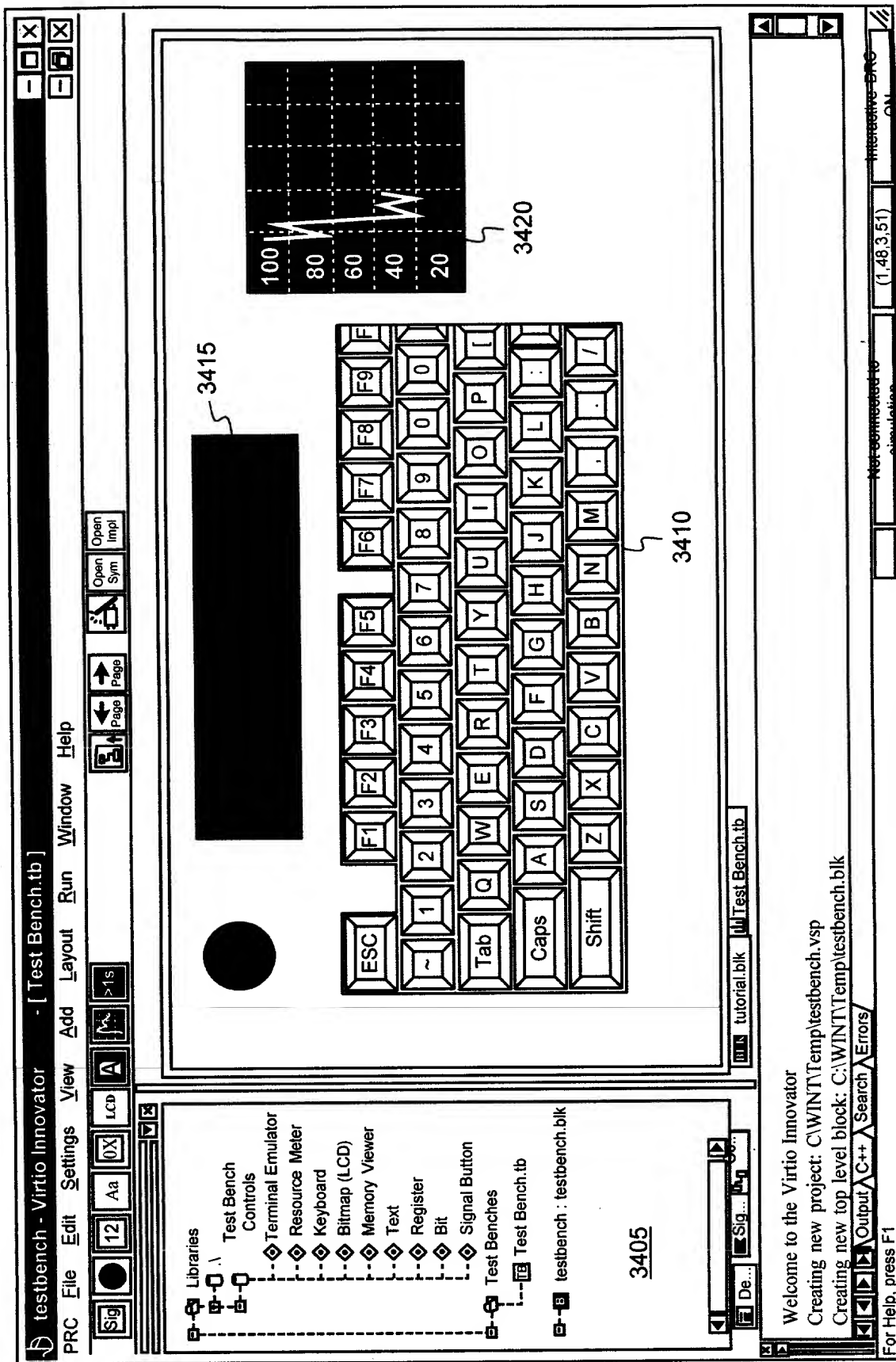


Fig. 34A

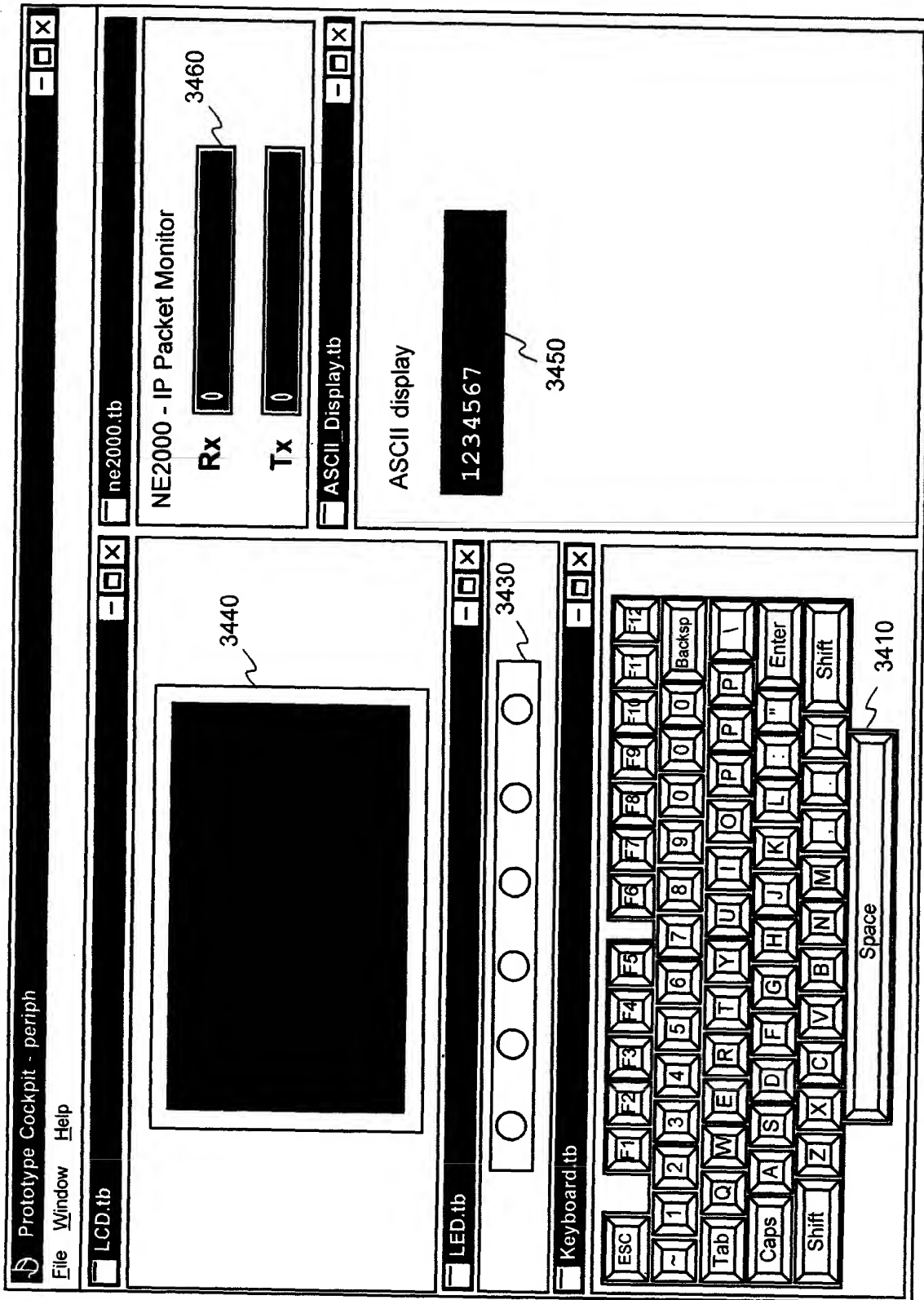
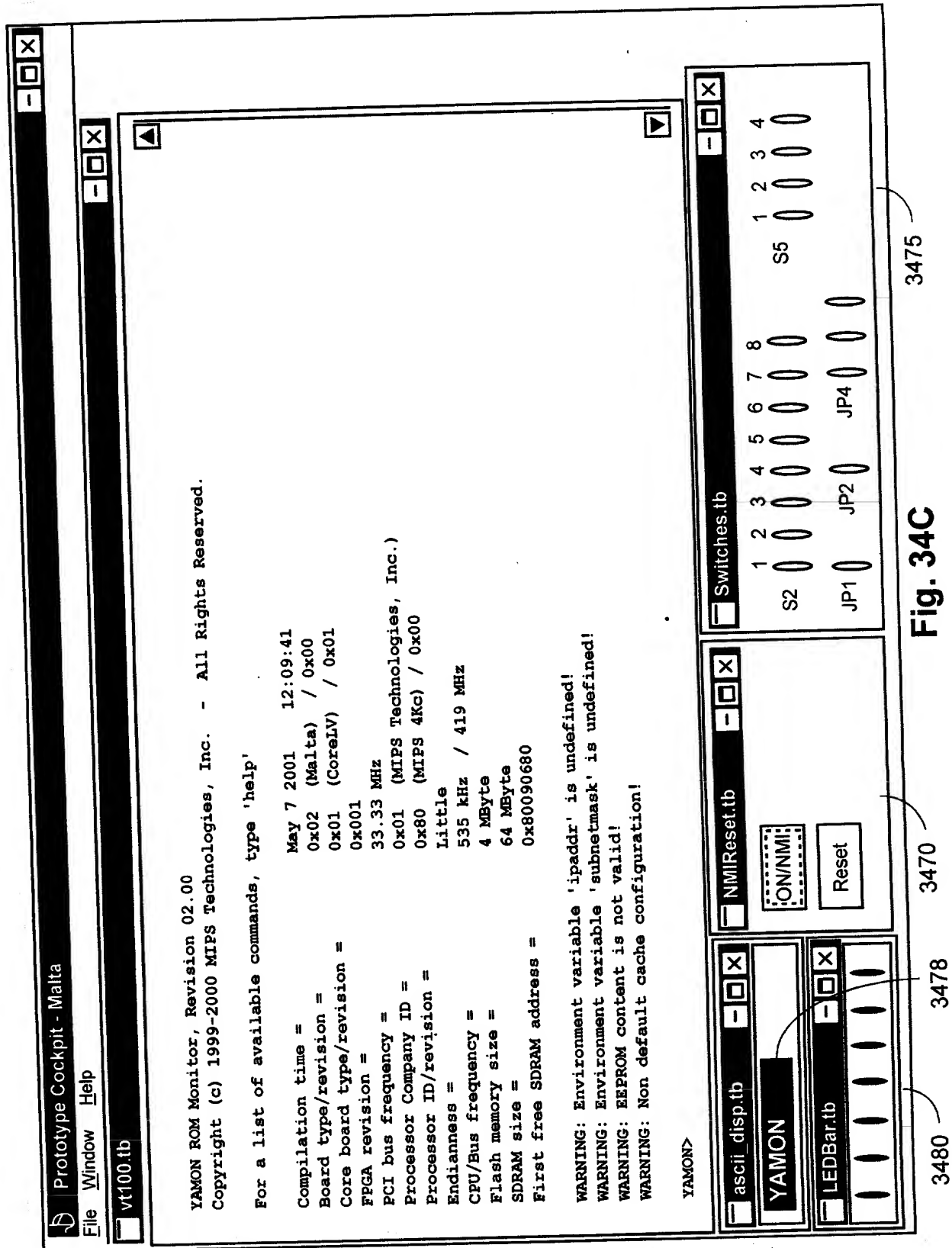


Fig. 34B



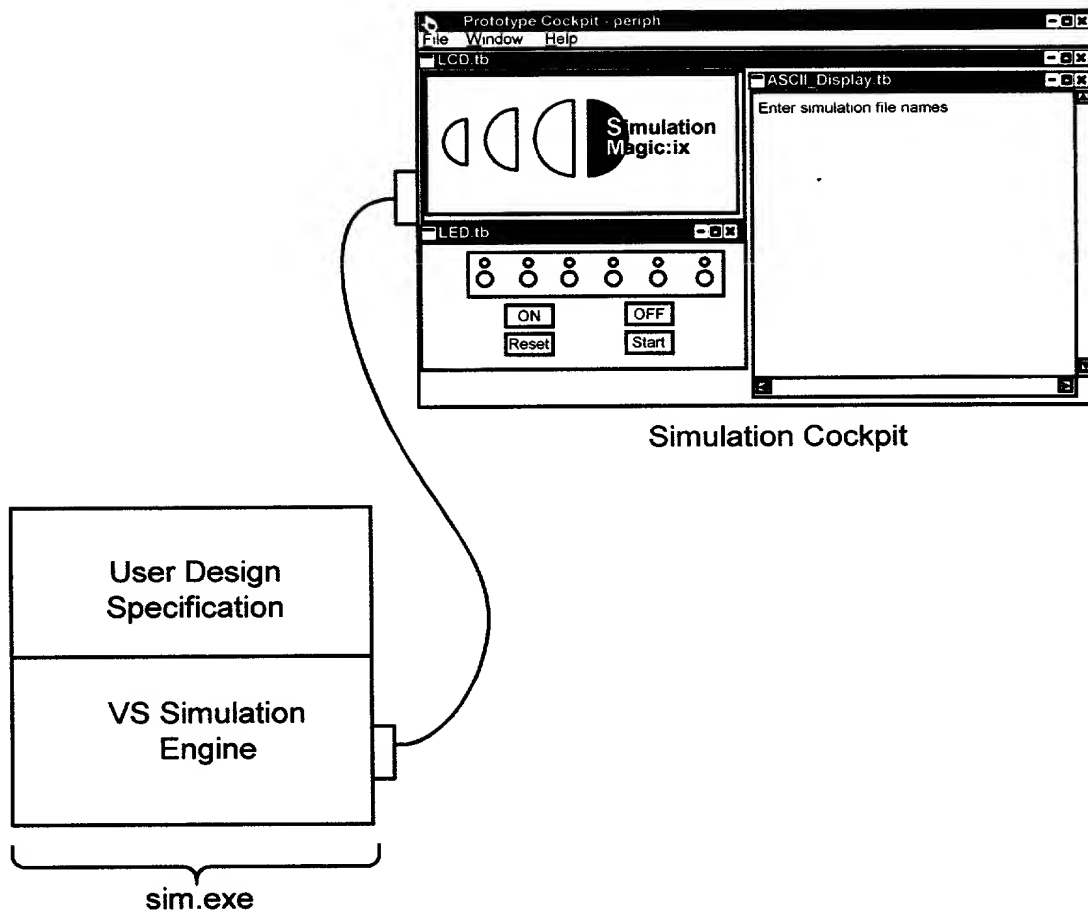
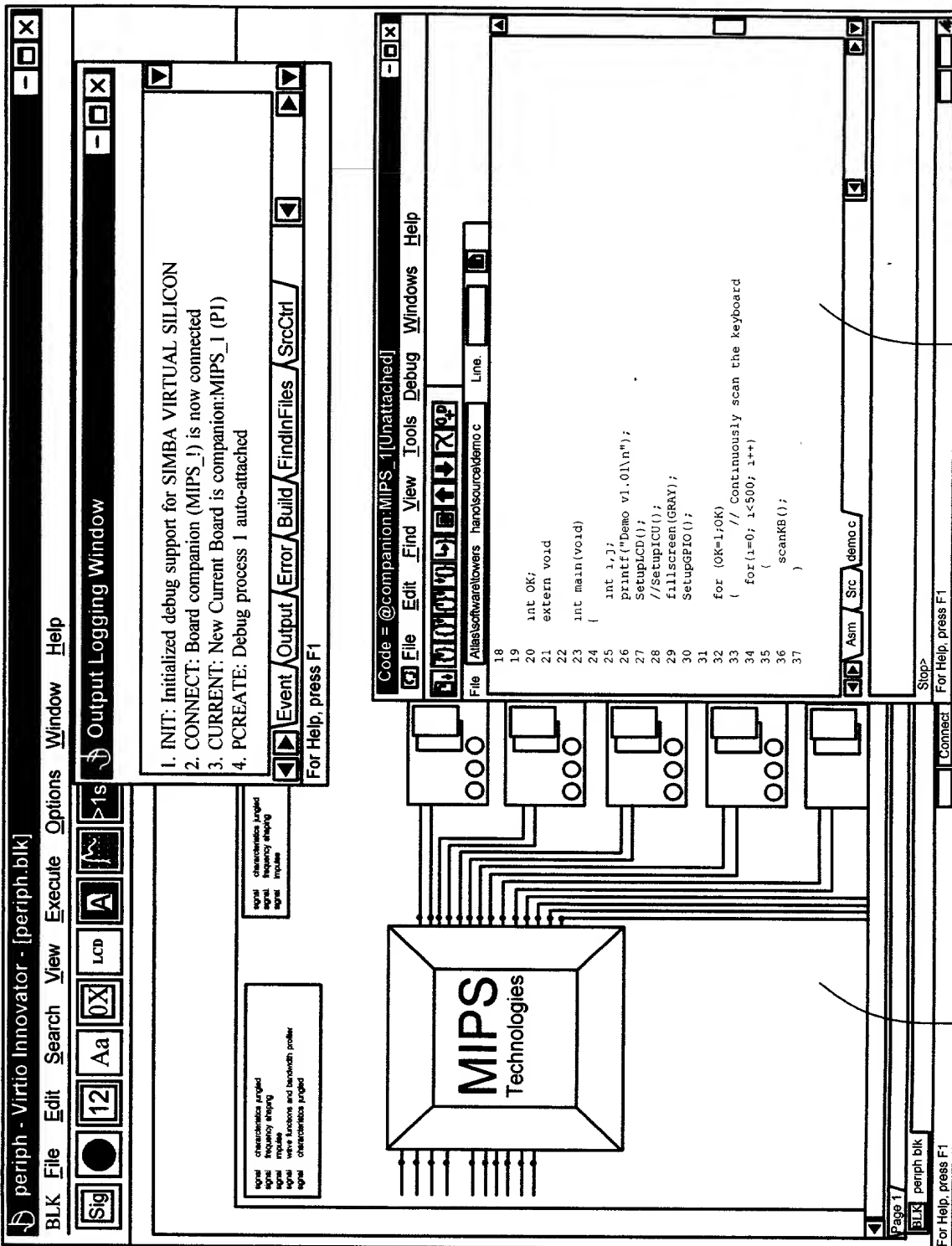


Fig. 35

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3620

Fig. 36B

3685

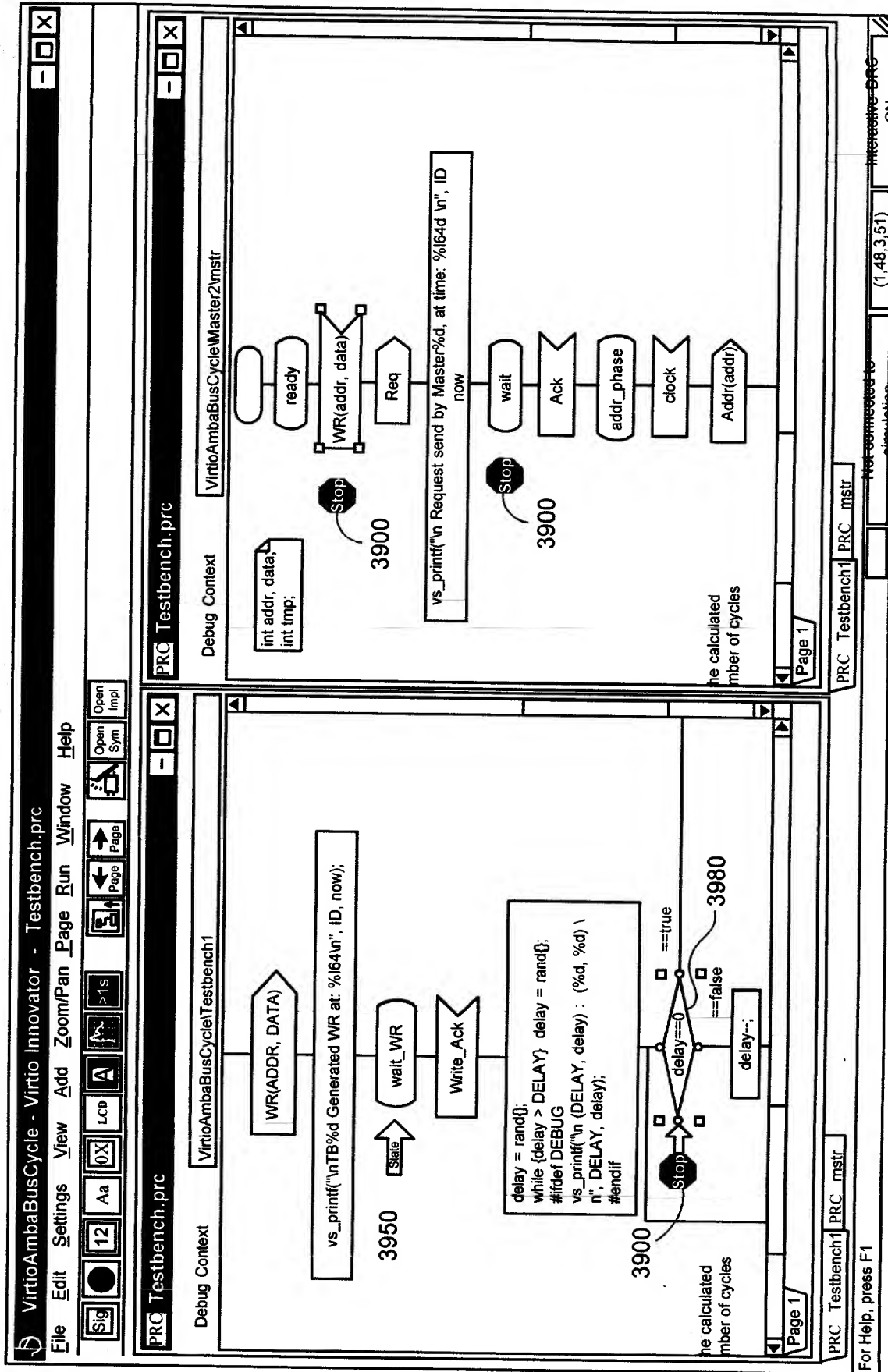


Fig. 36C

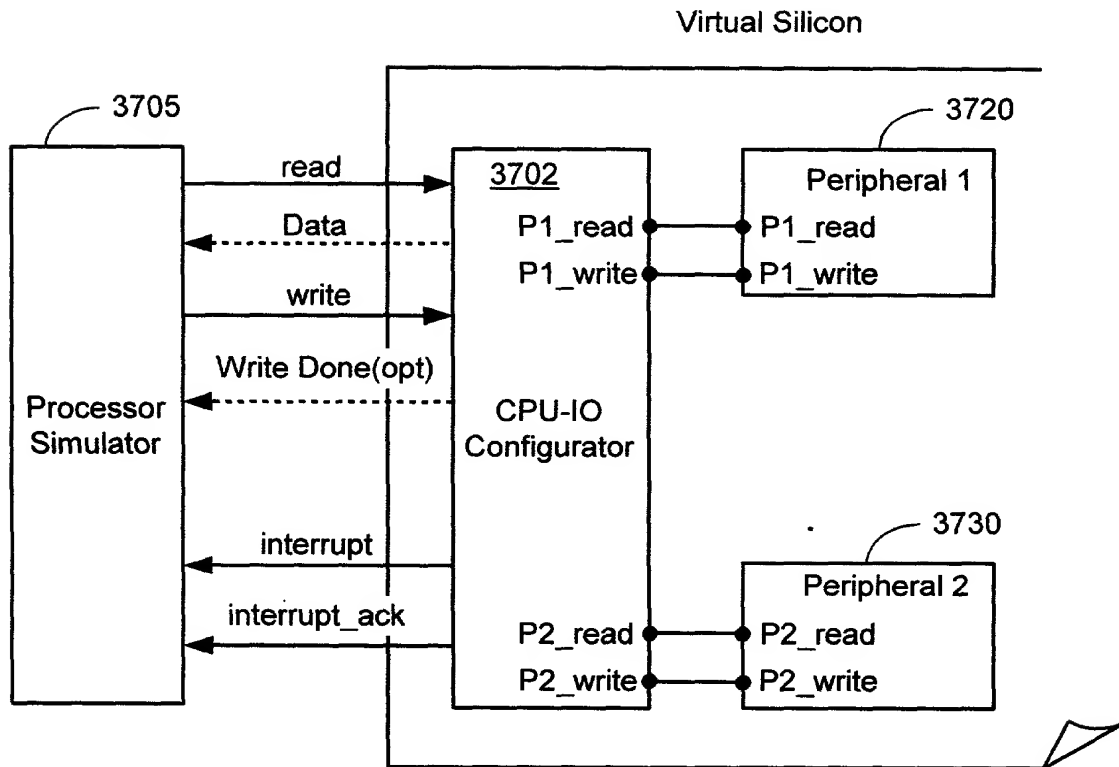


Fig. 37

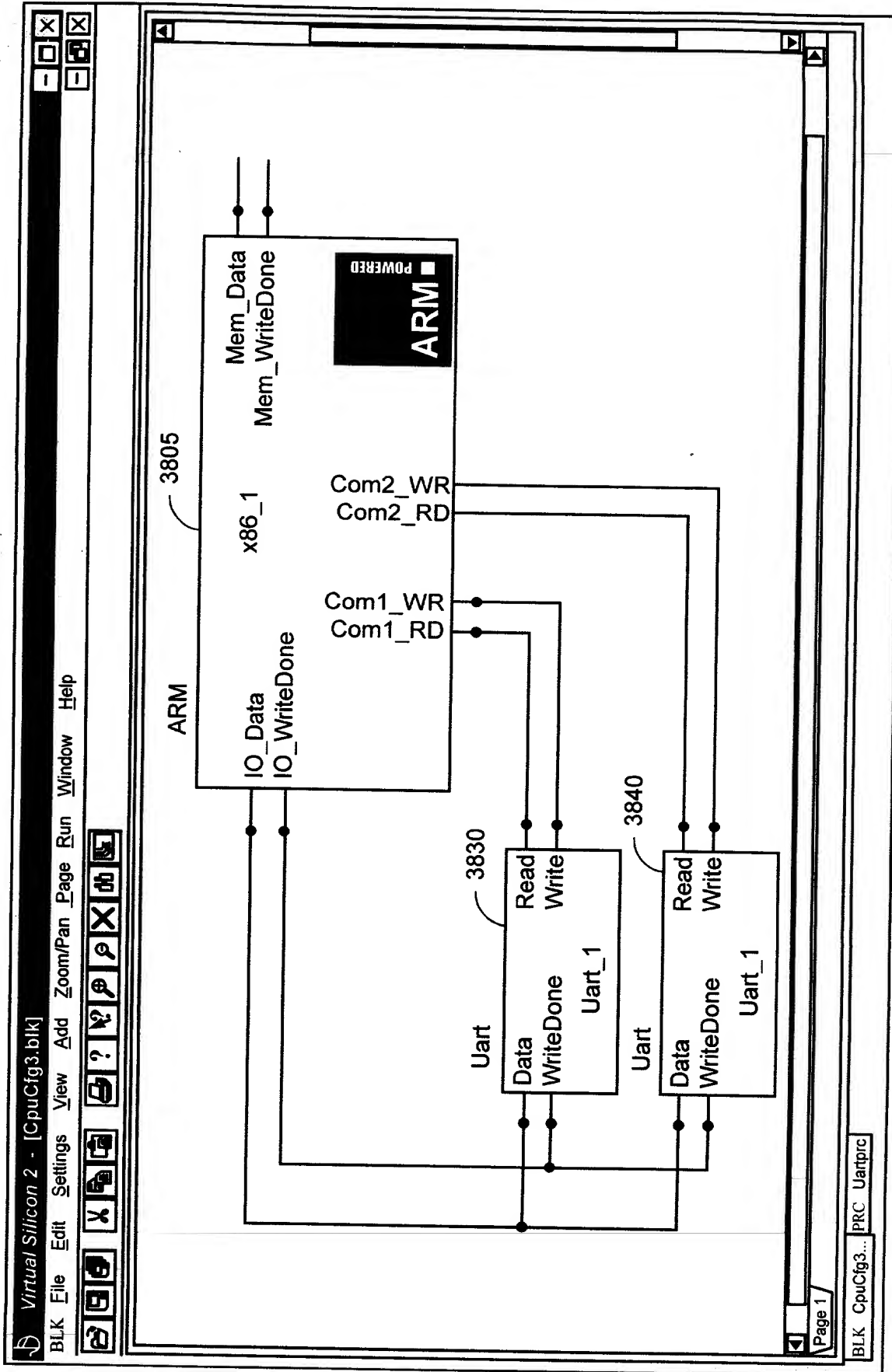


Fig. 38

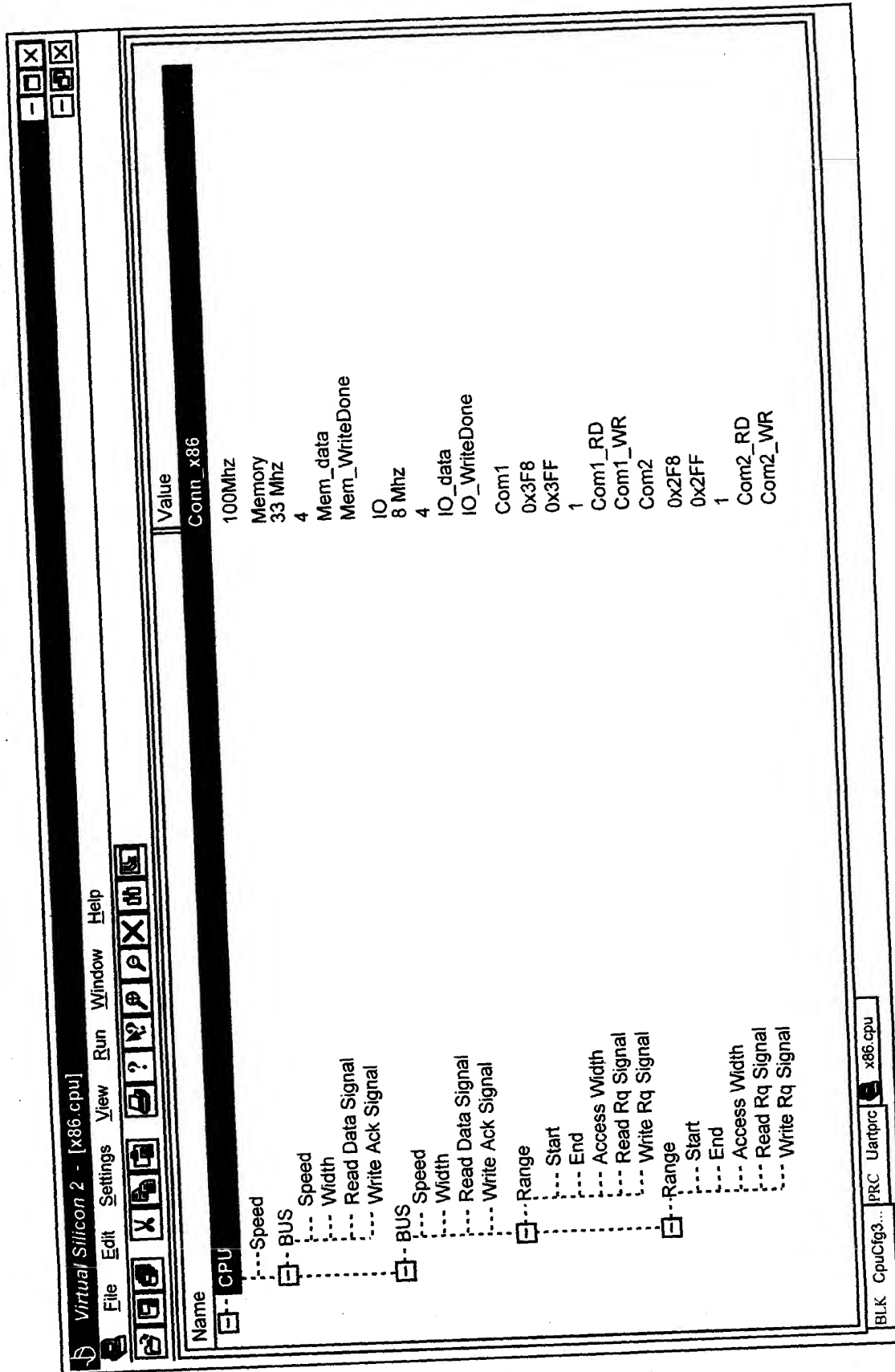
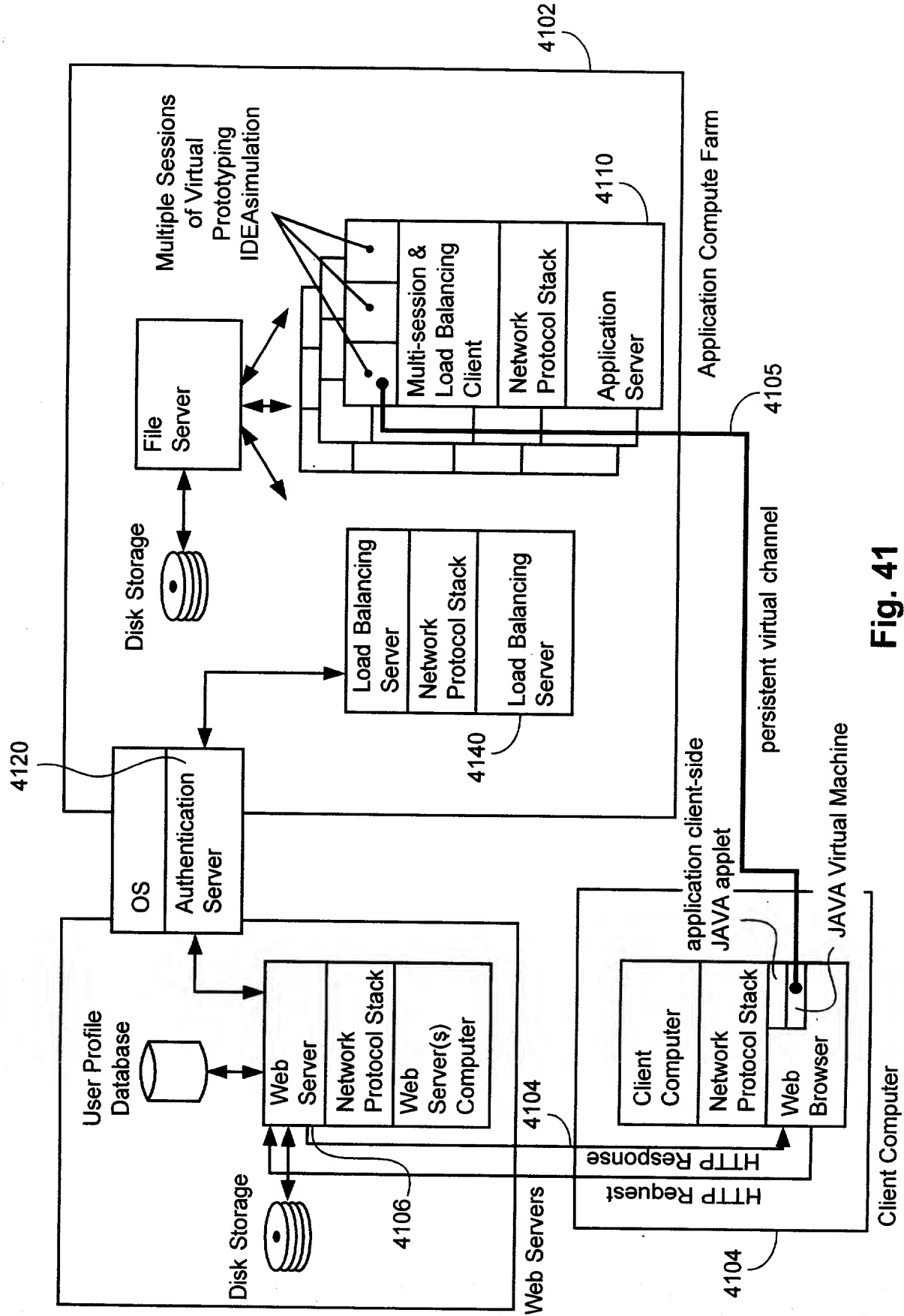


Fig. 39

Name	Value
<input checked="" type="checkbox"/> CPU	AmCPU
Speed	100Mhz
<input checked="" type="checkbox"/> Events: CPU -> Simulation	
Reset Signal	Rest
BUS_ACK Signal	Bus_ack
<input checked="" type="checkbox"/> Events: Simulation -> CPU	
BUS_RQ	Bus_RQ
<input checked="" type="checkbox"/> Interrupt Support	Yes
FIRQ Signal	FIQ
IRQ Signal	IRQ
<input checked="" type="checkbox"/> BUS	Memory
Speed	100Mhz
Width	4
Read Data Signal	Read_data
<input checked="" type="checkbox"/> Write Timing	Variable
Write Ack Signal	Write_Ack
<input checked="" type="checkbox"/> Range	Counter
Type	Slave
Start	CNT_START_ADDR
End	CNT_END_ADDR
Access Width	4
Read Rq Signal	CNT_RD
Write Rq Signal	CNT_WR

Fig. 40



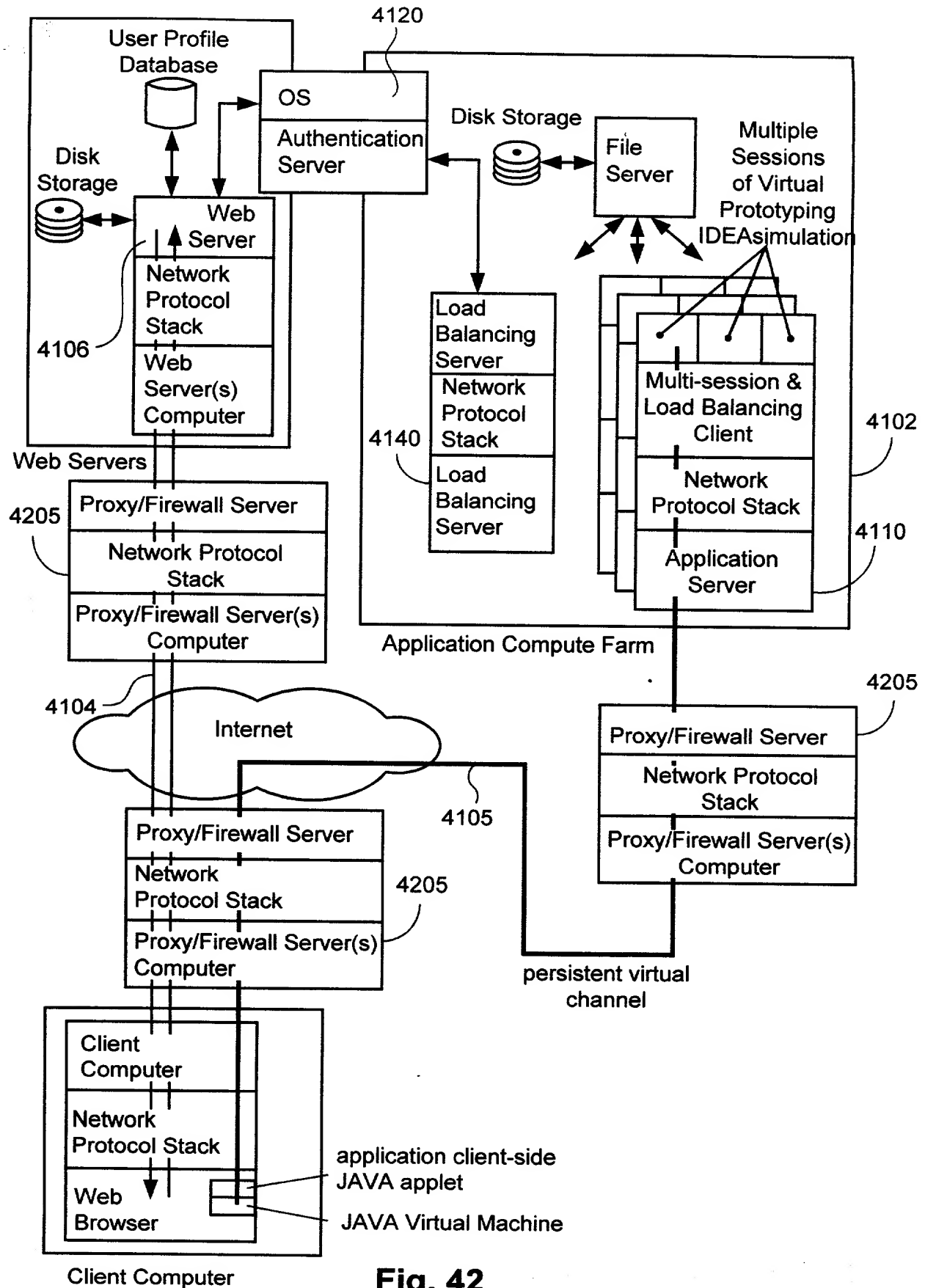


Fig. 42

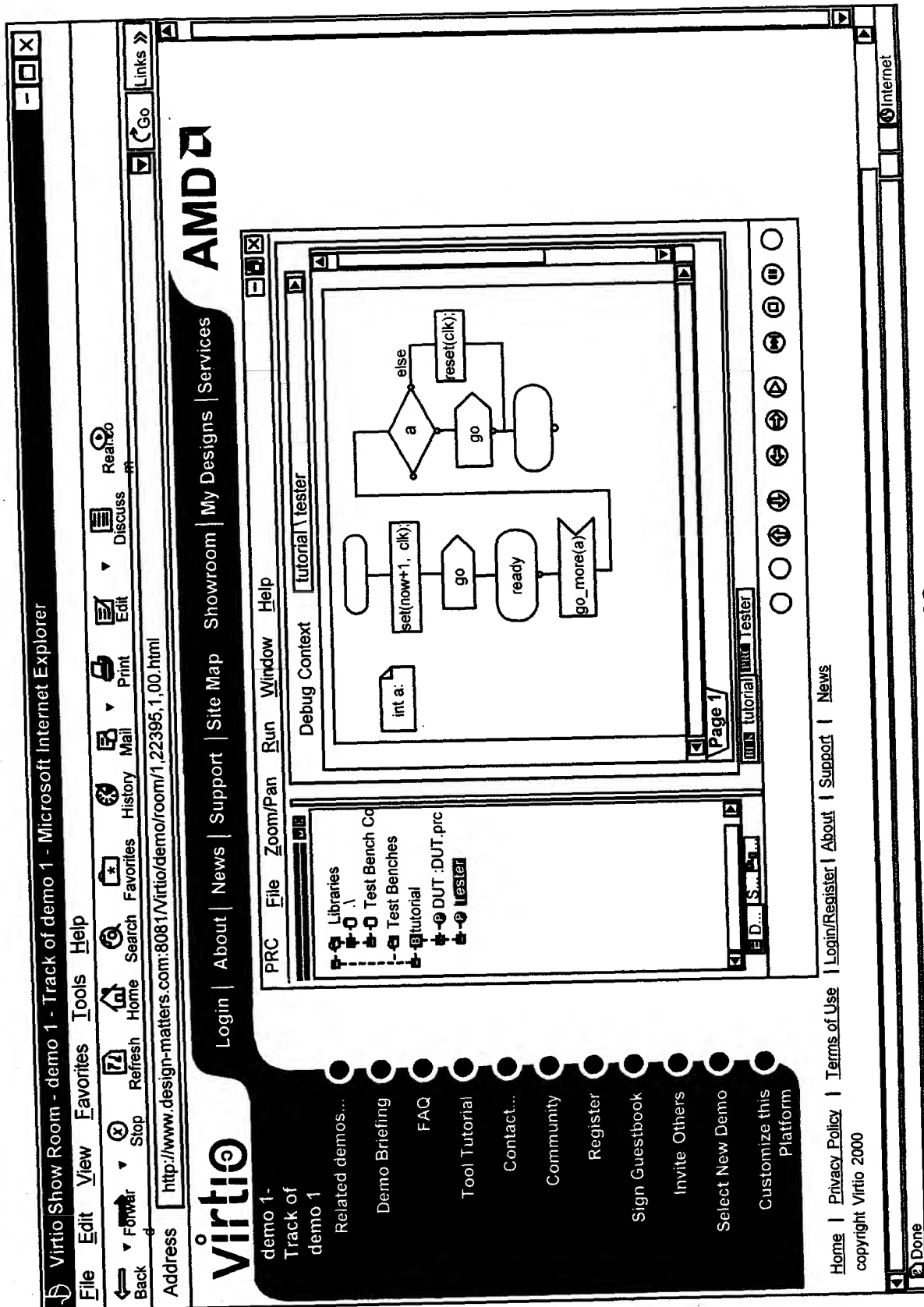


Fig. 43

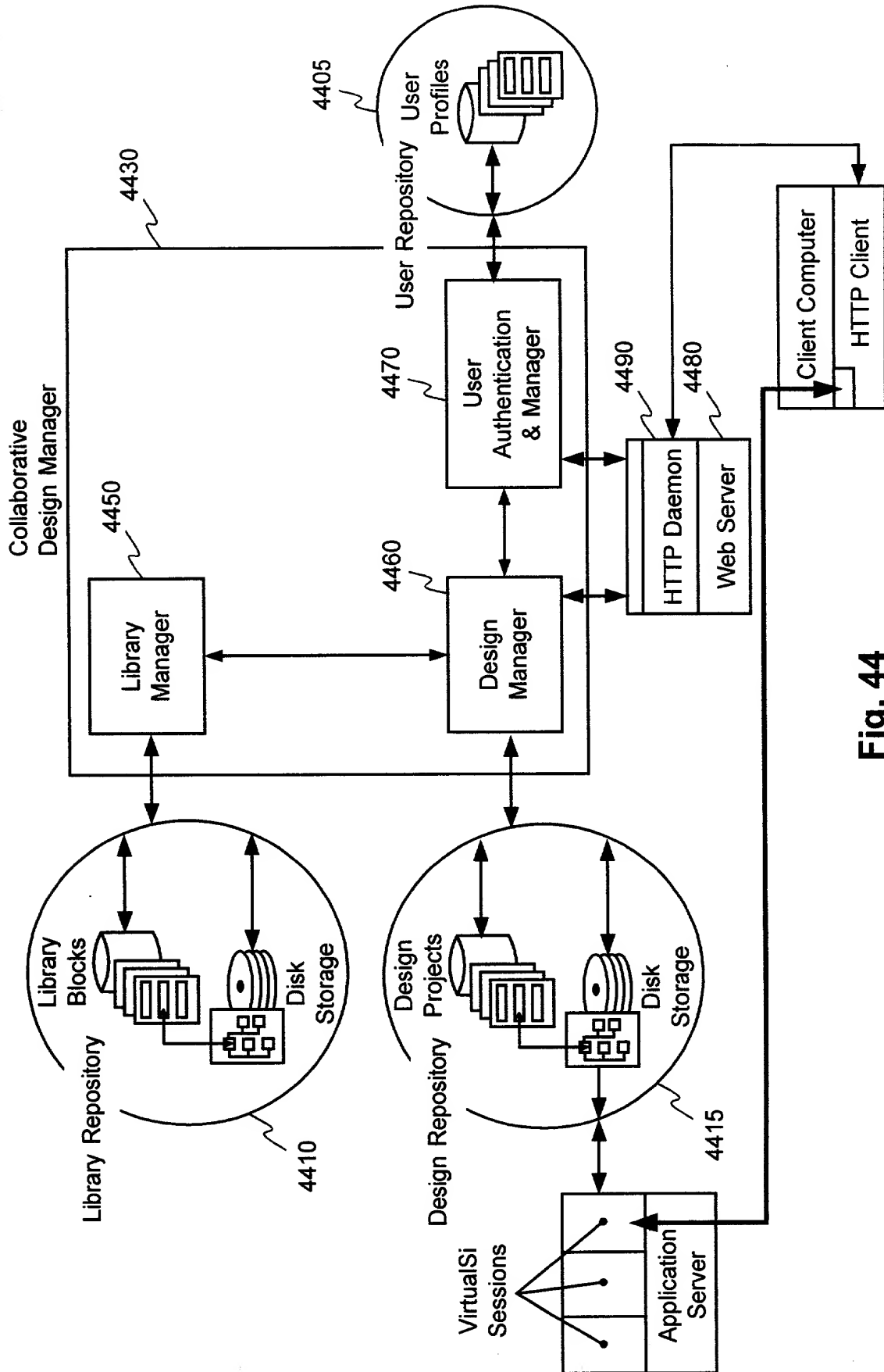




Fig. 44

 Clock_1	Scope Name
 clk(int)	Signal name and declaration







 t	Timer or clock name and declaration
S clk	Local name of a signal coming from the upper scope (inherited)
 myClk 	Timer or clock is being set
	Signal is being sent
	Signal is being received
	Signal is being saved

Fig. 45

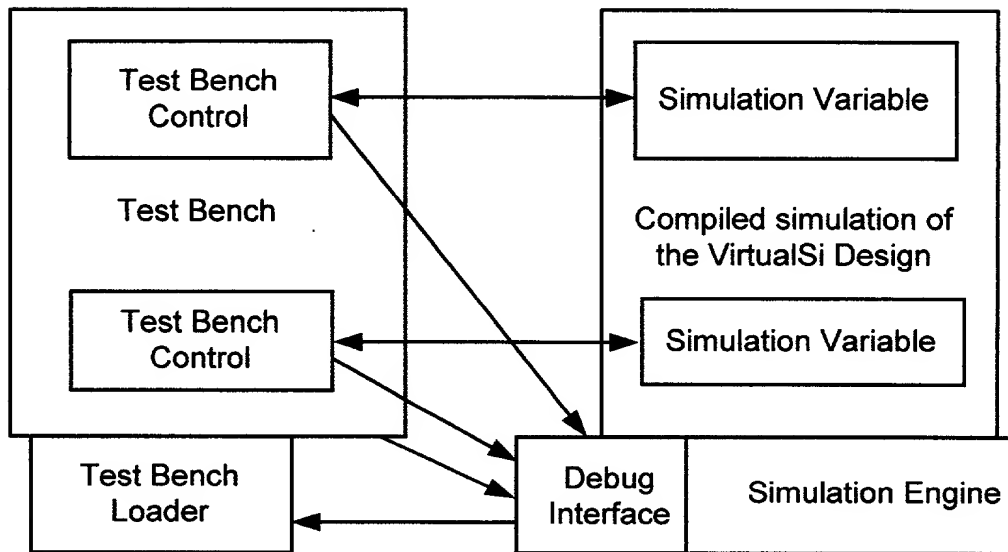


Fig. 46

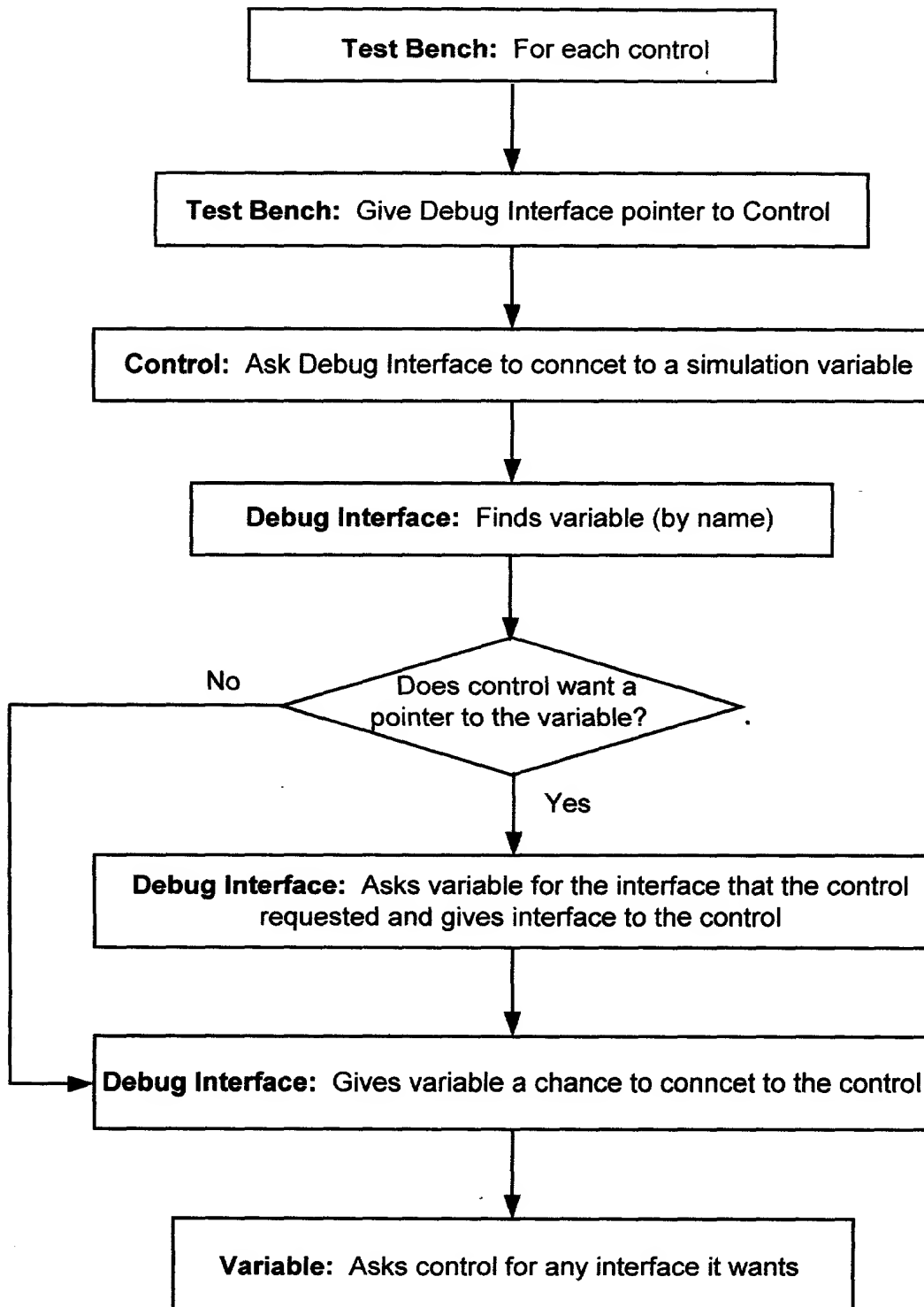


Fig. 47

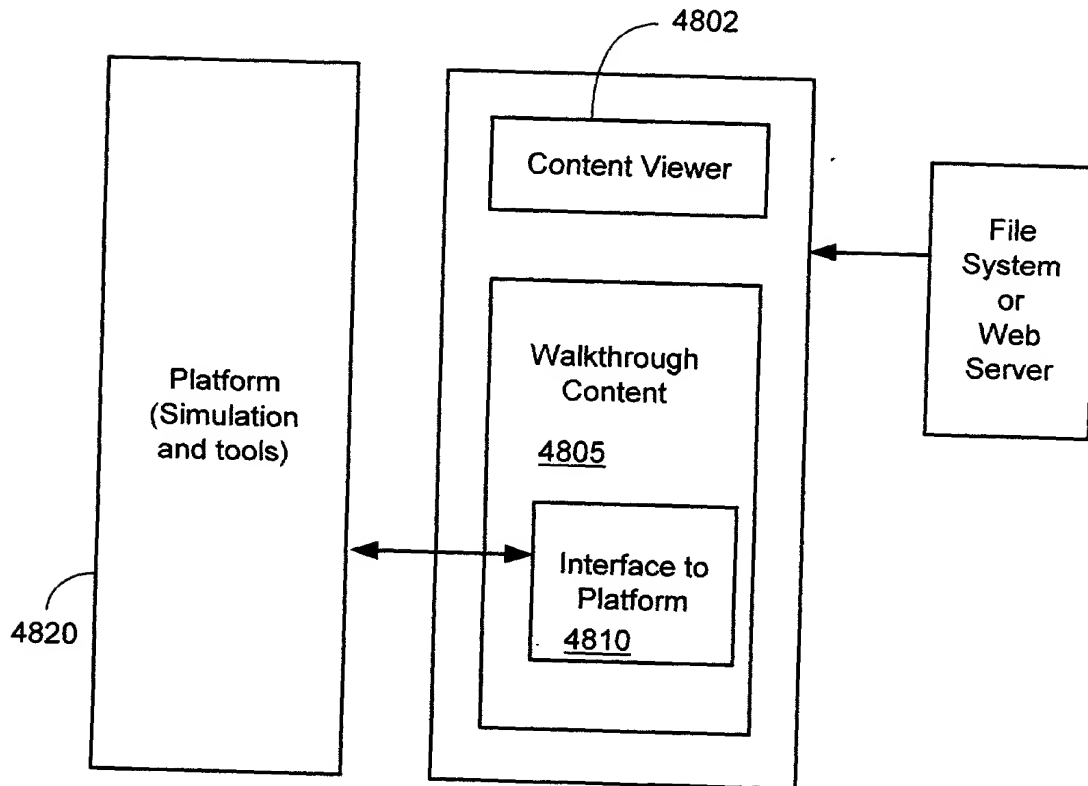


Fig. 48

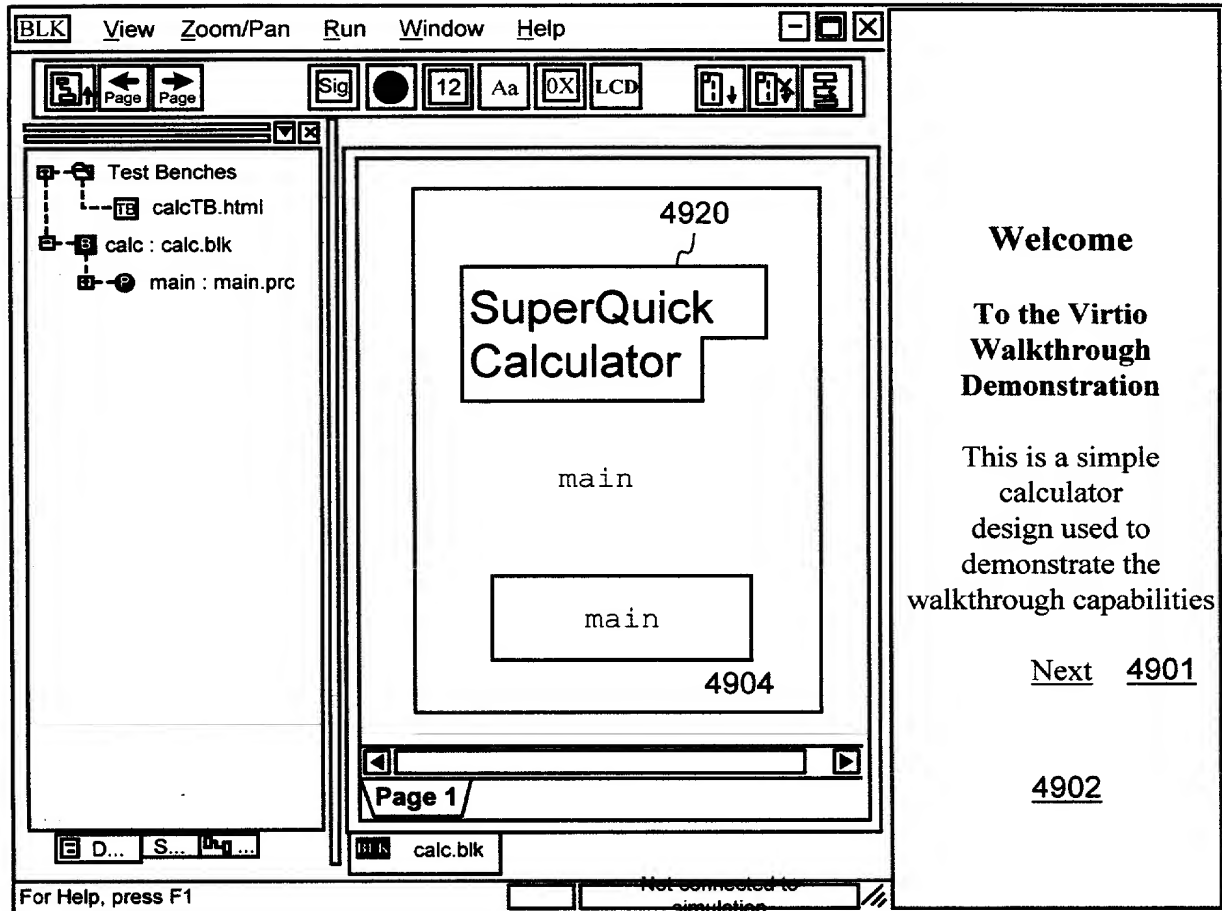


Fig. 49A

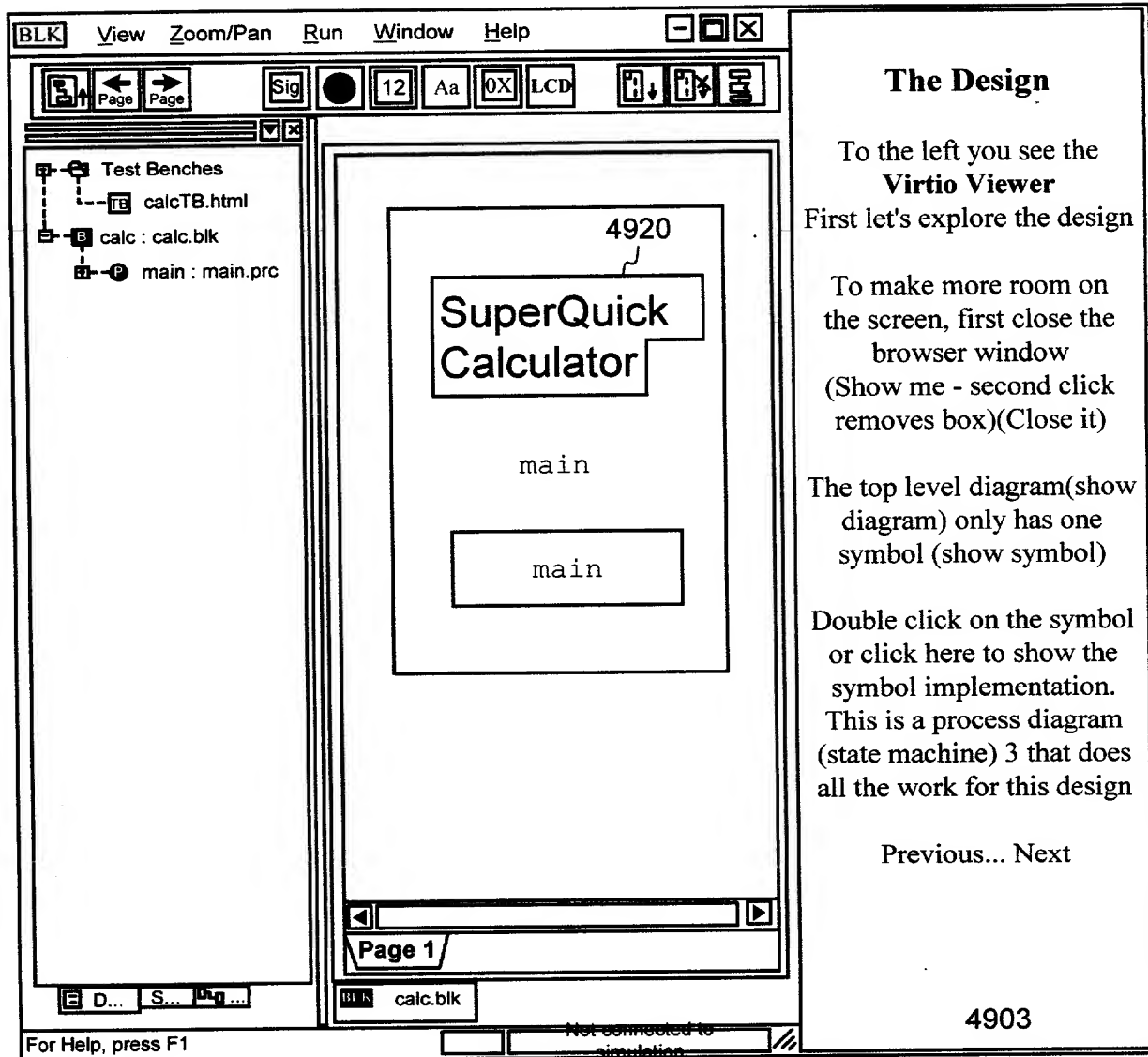


Fig. 49B

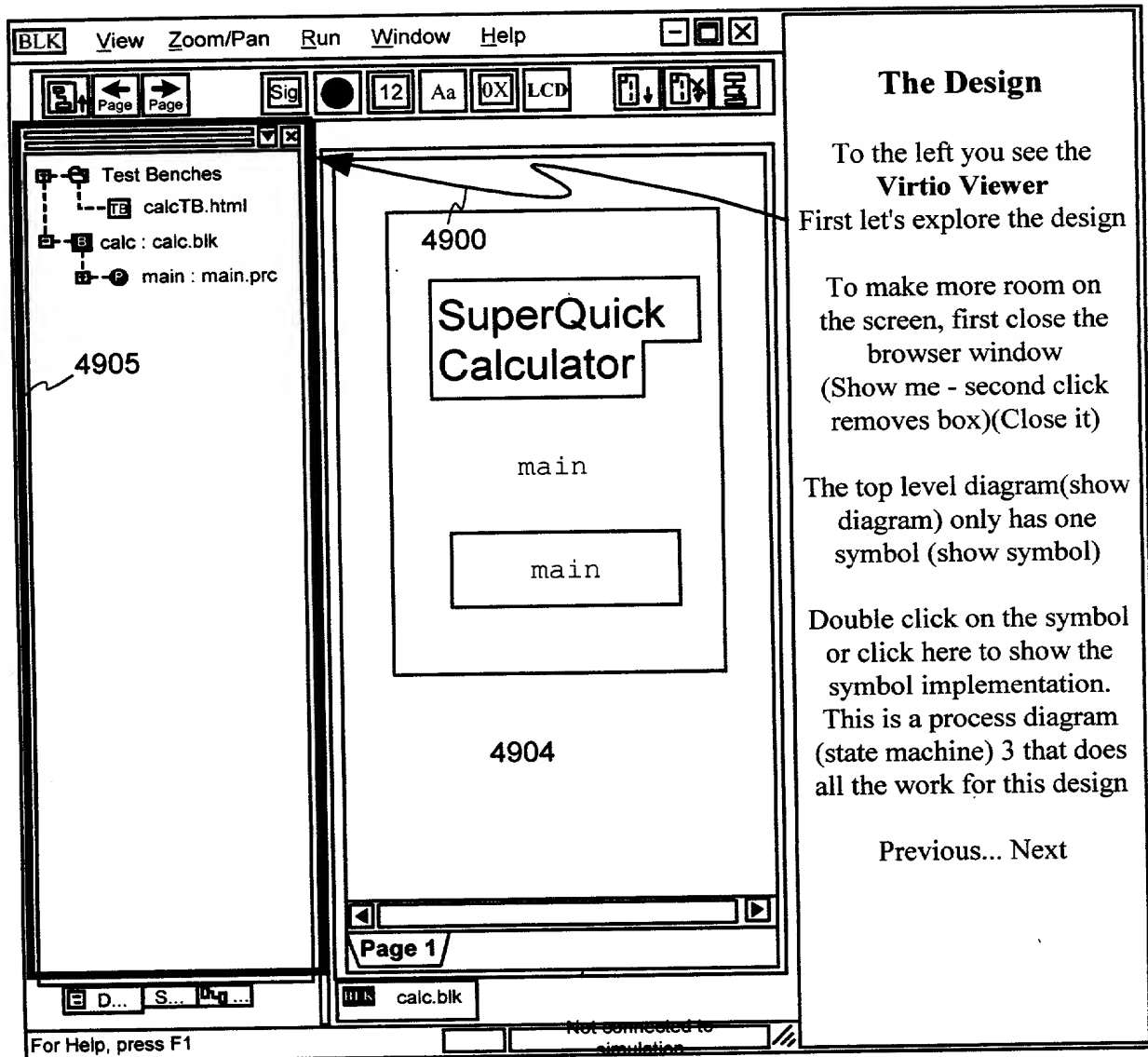
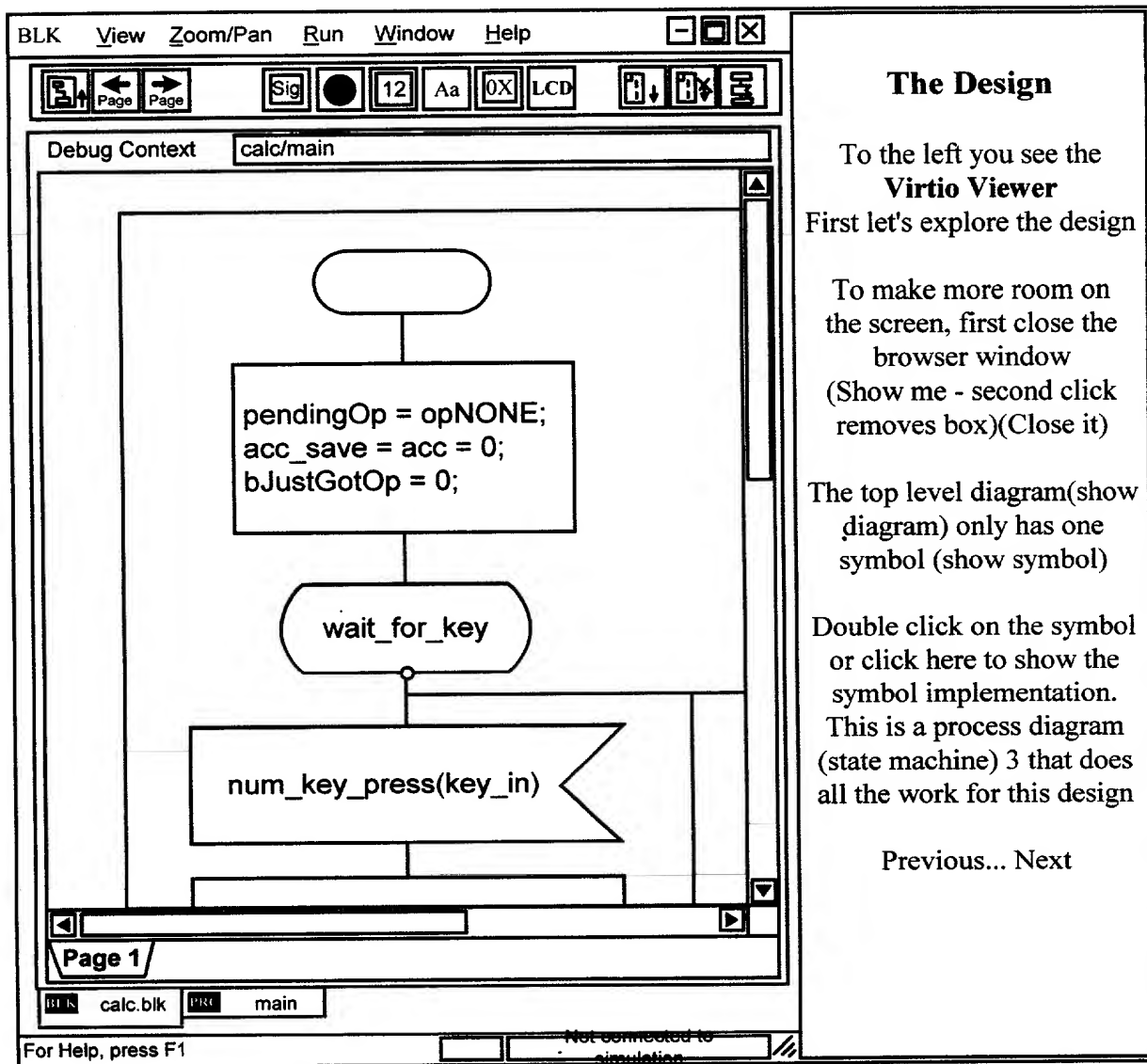


Fig. 49C



The Design

To the left you see the
Virtio Viewer
 First let's explore the design

To make more room on
 the screen, first close the
 browser window
 (Show me - second click
 removes box)(Close it)

The top level diagram(show
 diagram) only has one
 symbol (show symbol)

Double click on the symbol
 or click here to show the
 symbol implementation.
 This is a process diagram
 (state machine) 3 that does
 all the work for this design

Previous... Next

Fig. 49D

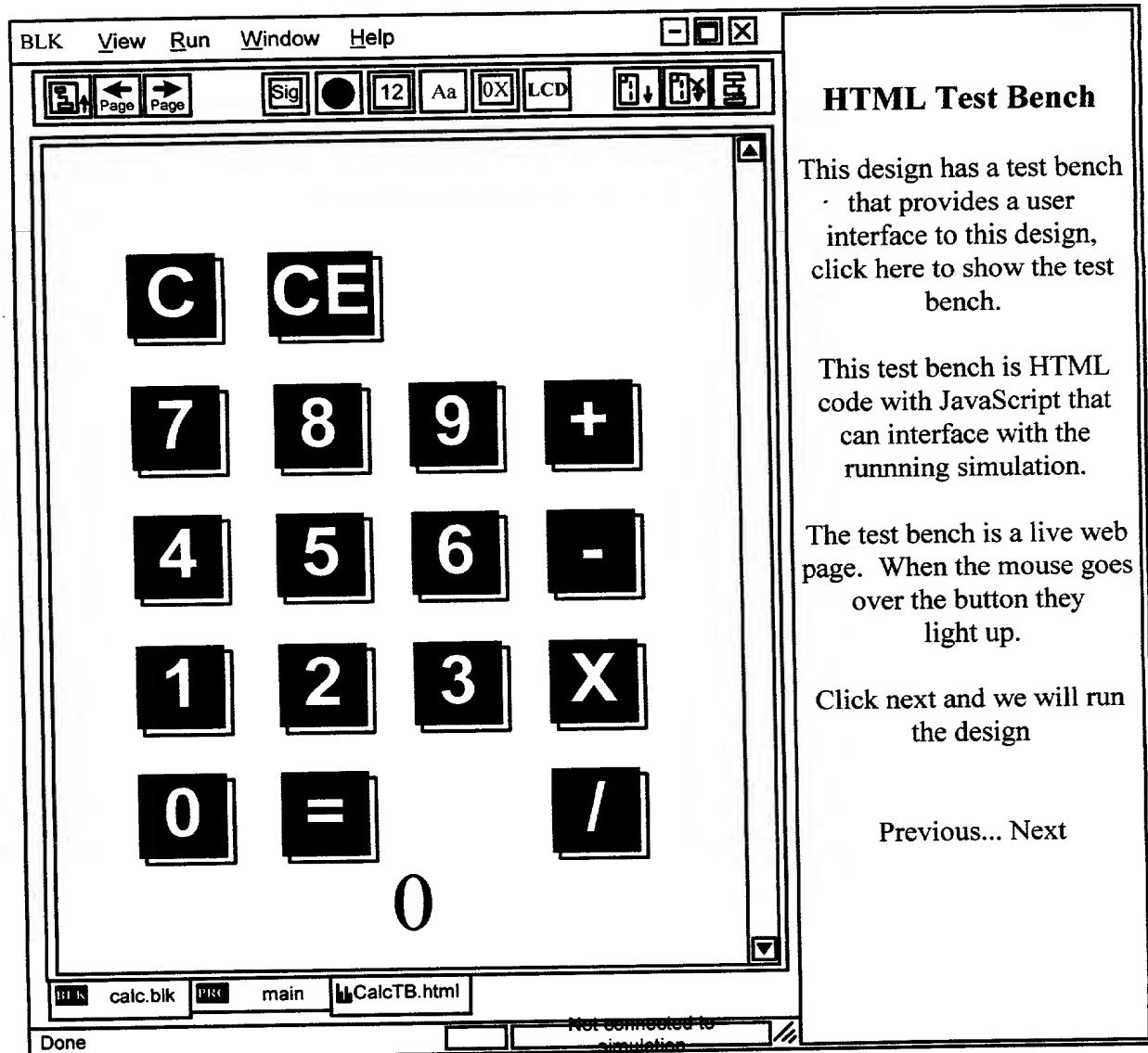


Fig. 49E

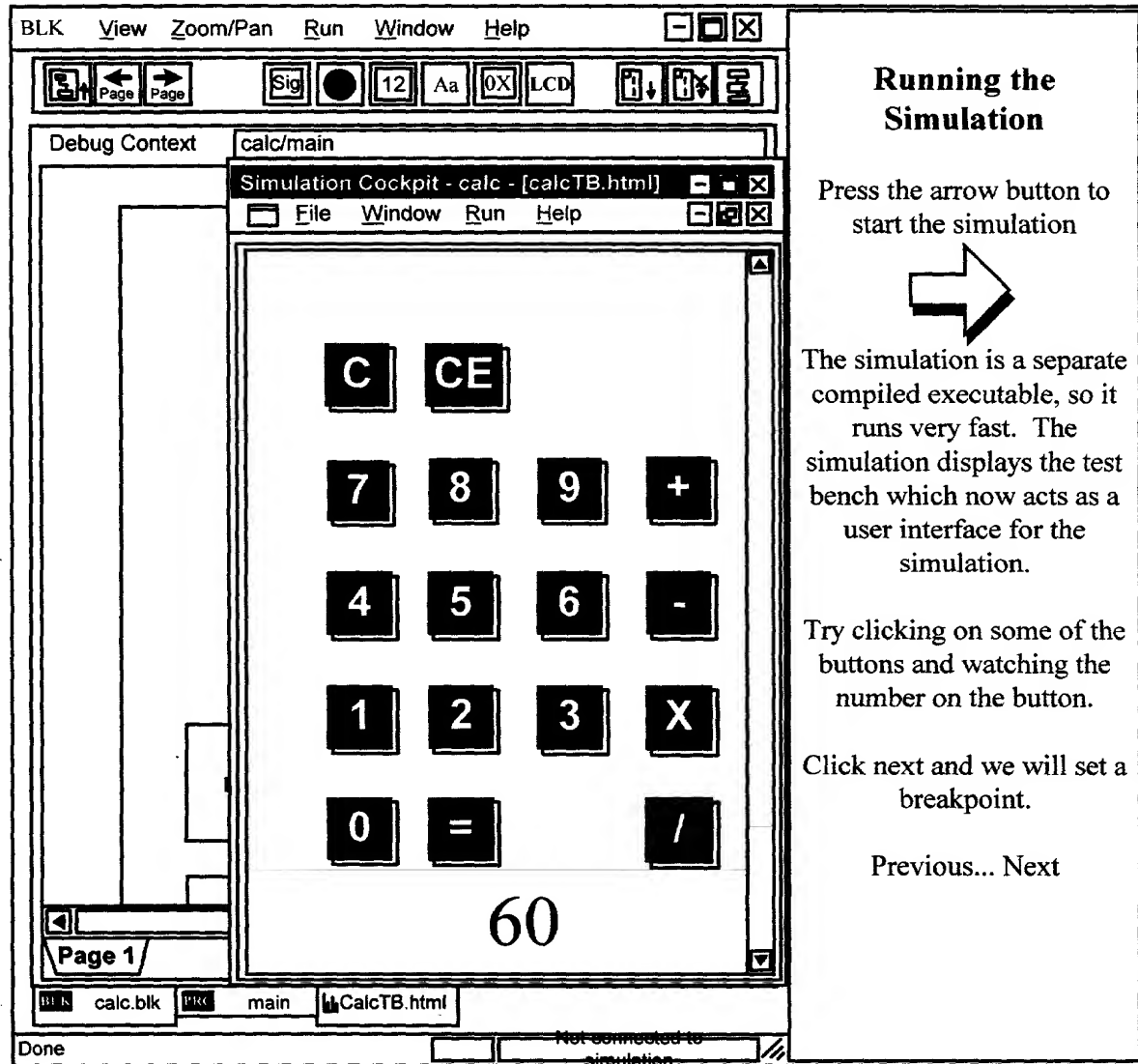


Fig. 49F

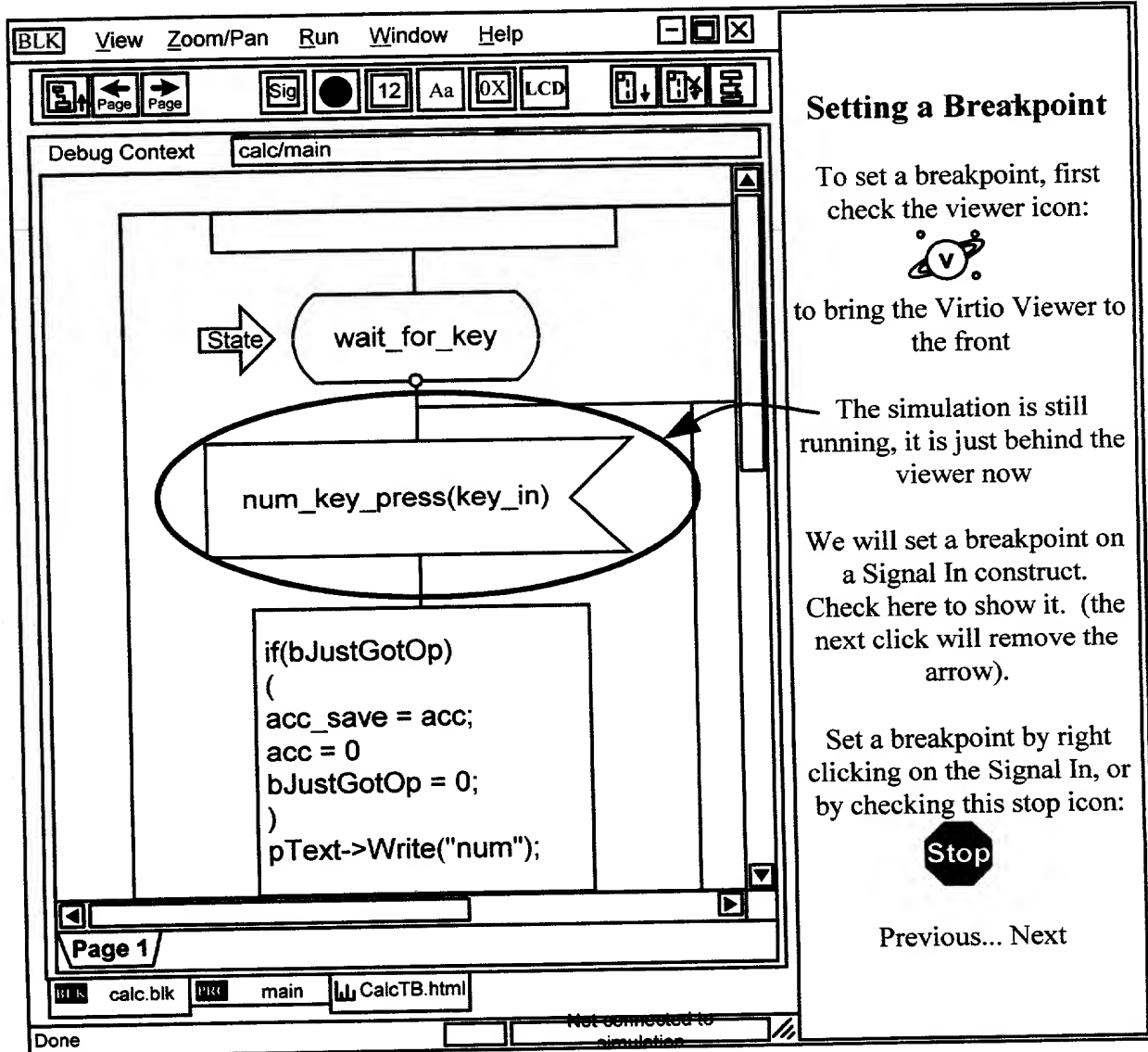


Fig. 49G

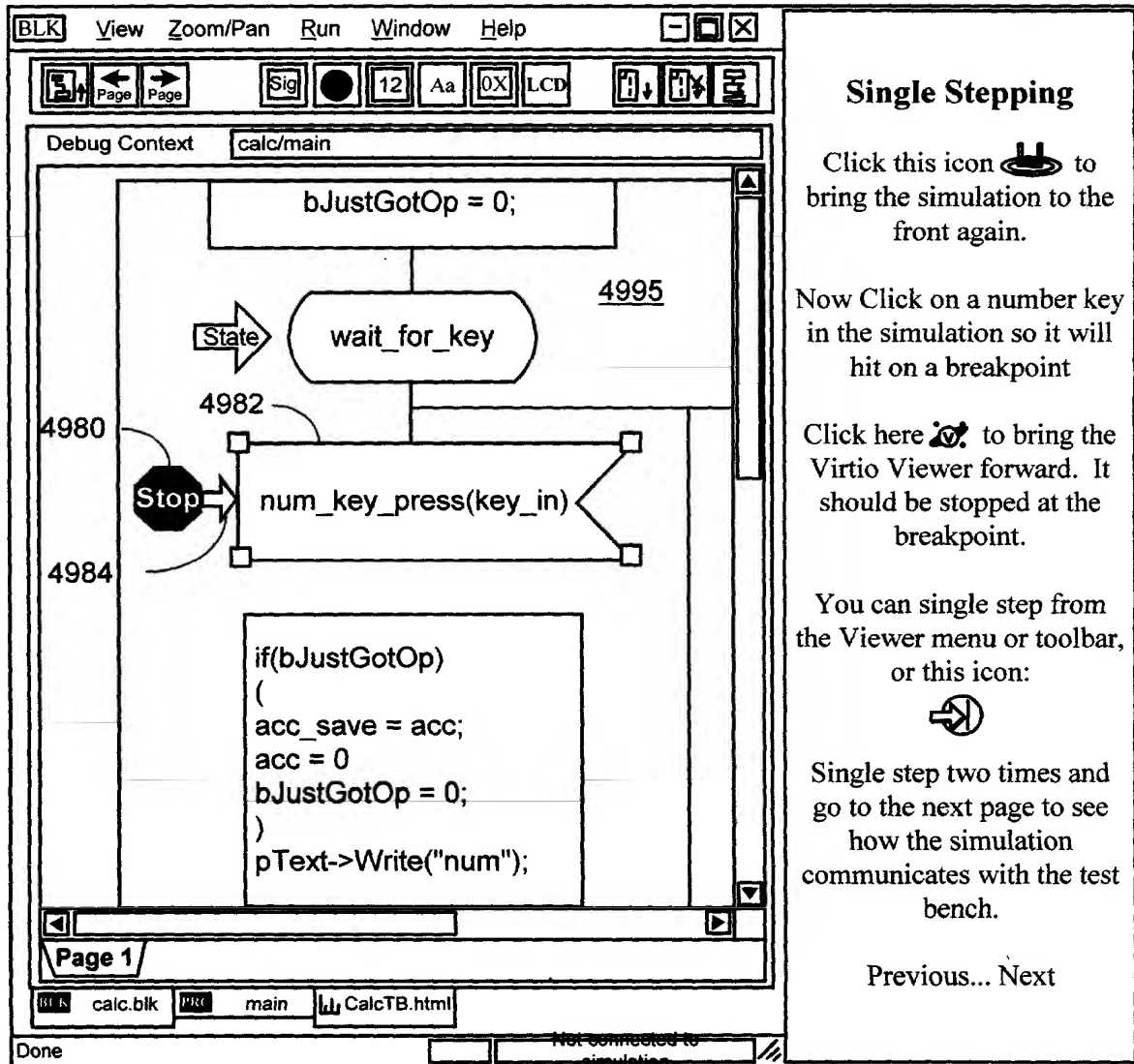


Fig. 49H

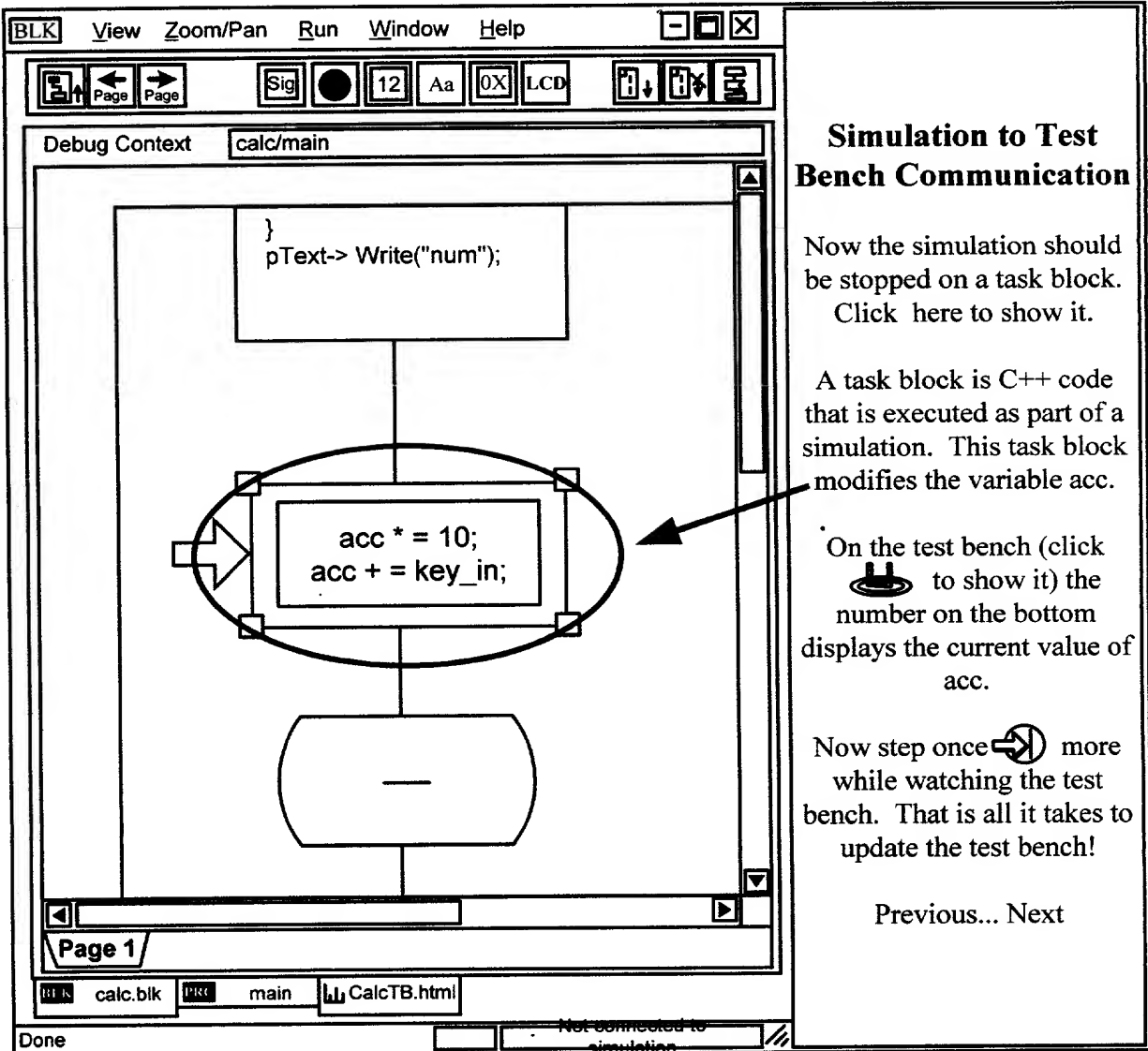


Fig. 49I

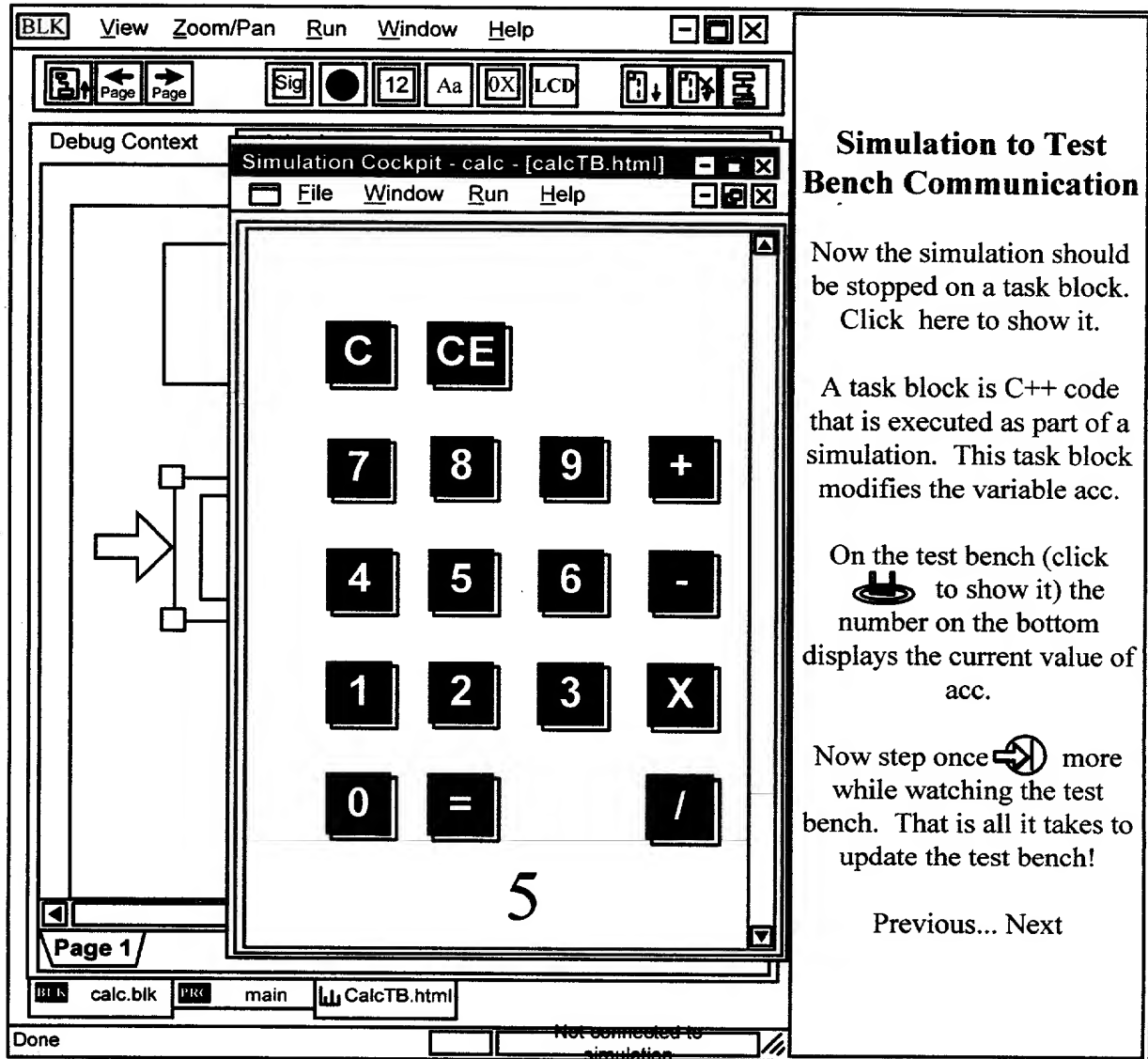


Fig. 49J

Integrator Lab Screen Snap Shots - On-Line Enablement

Virtio OnLine - Integrator Lab - Microsoft Internet Explorer

File Edit View Favorites Tools Help

Back Forward Stop Refresh Home Search Favorites History Mail Print Edit Discuss Real.c

Address <http://www.virtio.com/online/integrator/0,2263,0,00.html> Go Links Redherring.com

Home Logout Feedback SiteMap

virtio About Newsroom Technology Support **Virtio Online** Partners

Explorer Studio Integrator Lab Platform Publisher

Virtio Virtio OnLine Integrator Lab

Integrator Lab

Current Designs Browse IP

<u>Design Name</u>	<u>Creation Date</u>	<u>Last Edit Date</u>	<u>Description</u>	Delete Project
<u>test</u>	02-May-01	29-May-01	test	Delete
<u>pcnetlink</u>	04-May-01	25-May-01	asdasd	Delete
<u>clonetutorial</u>	23-May-01	23-May-01	testing cloning of build77	Delete
<u>clonehanoi</u>	25-Apr-01	31-May-01	cloning hanoi	Delete
<u>cloneatlas</u>	25-Apr-01	29-May-01	cloning atlas	Delete

New Design My Invitees

Fig. 50

Design Wizard - Setup New Design (Step 1) - Microsoft Internet Explorer

Virtio
Integrator Lab

Step 1
Setup New Design
Please fill in the name and description for the new design

Setup New Design

Please provide a name and description for your new design

NOTE: Design names must start with a letter and may only contain alpha or numeric characters

Design Name 5110
dvd

Description 5115
MIPS32KC-based DVD setup box

Start by cloning an existing platform:

Clone 5120

5105

5102

Fig. 51

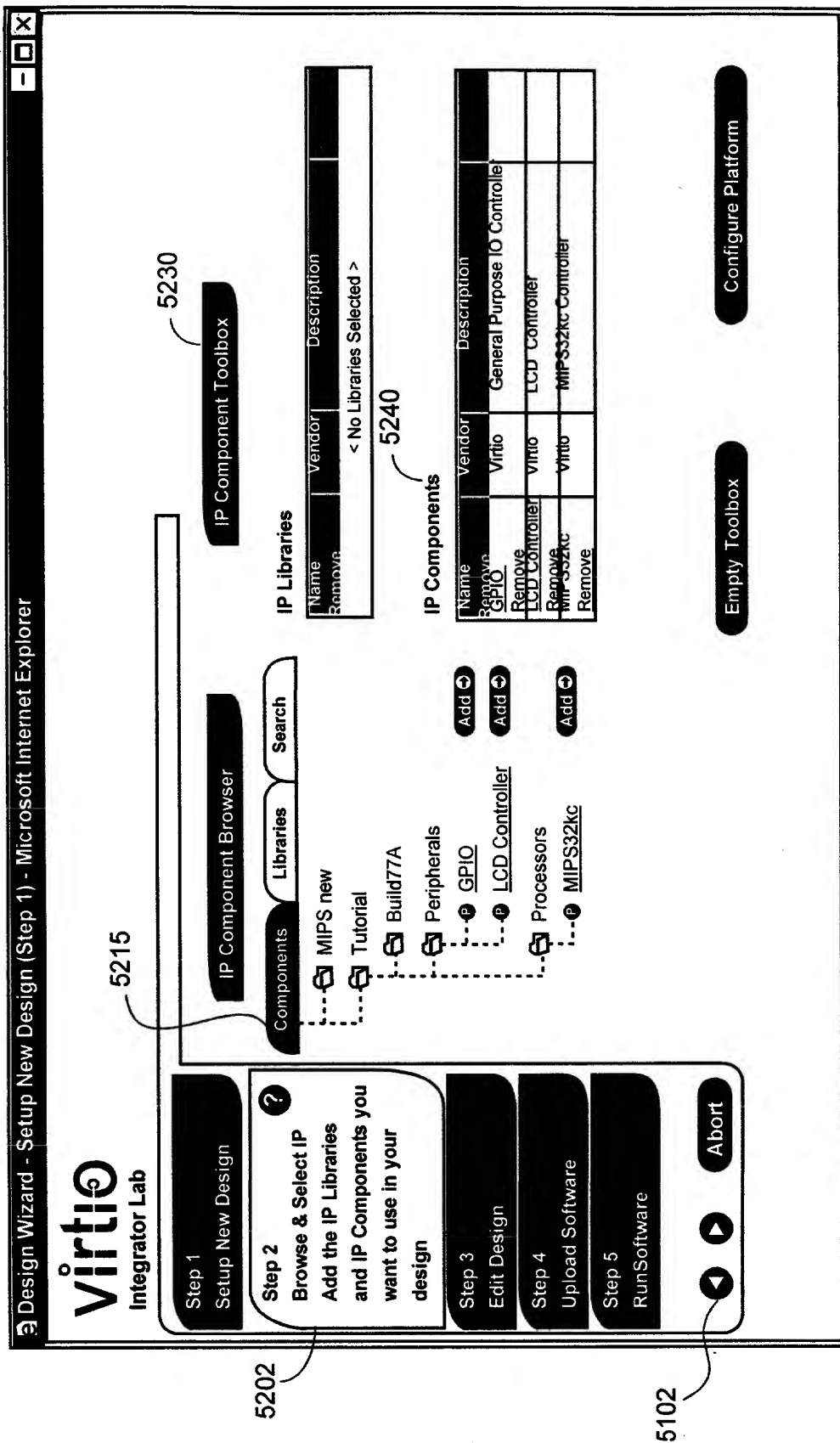


Fig. 52

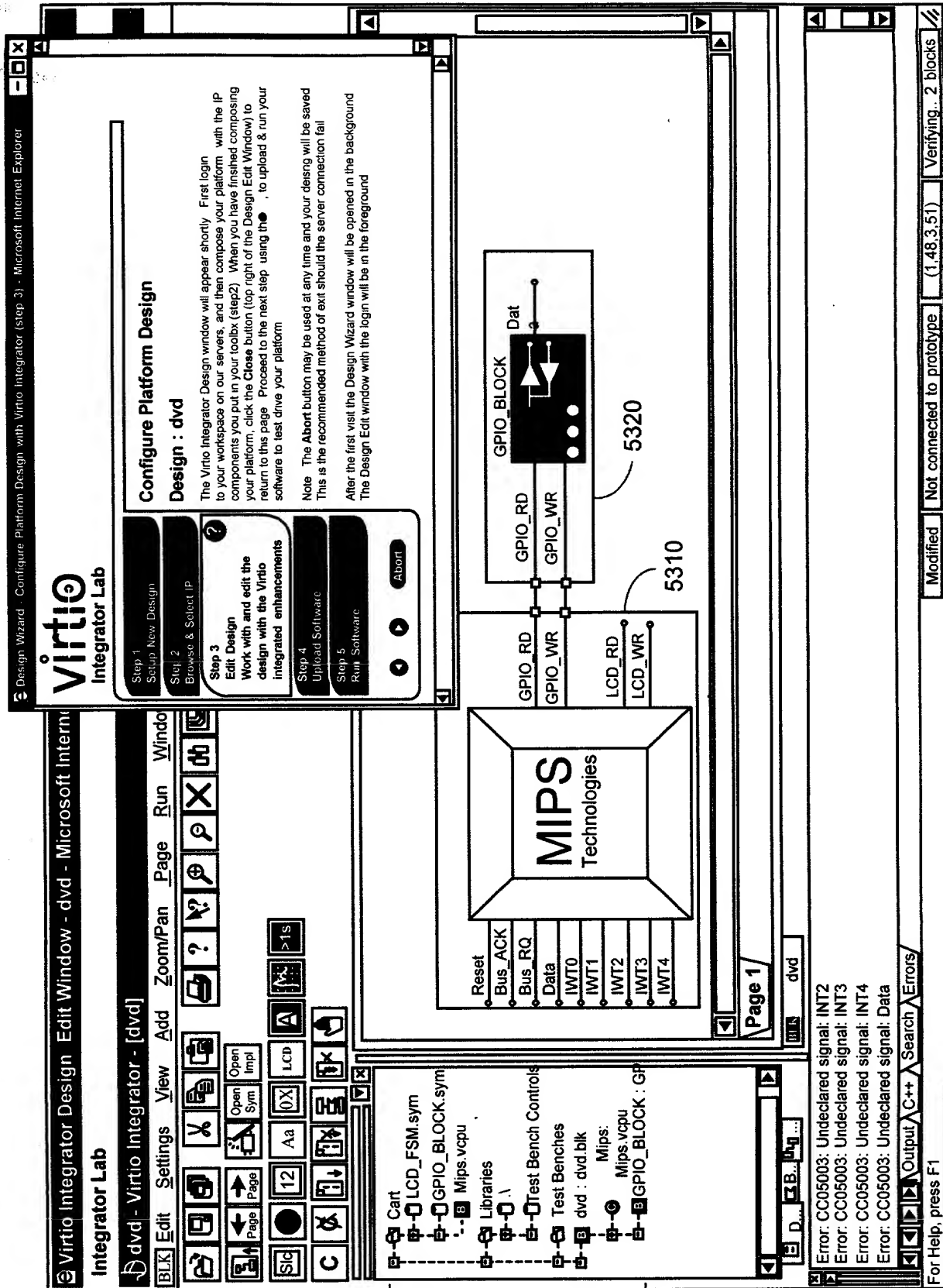


Fig. 53

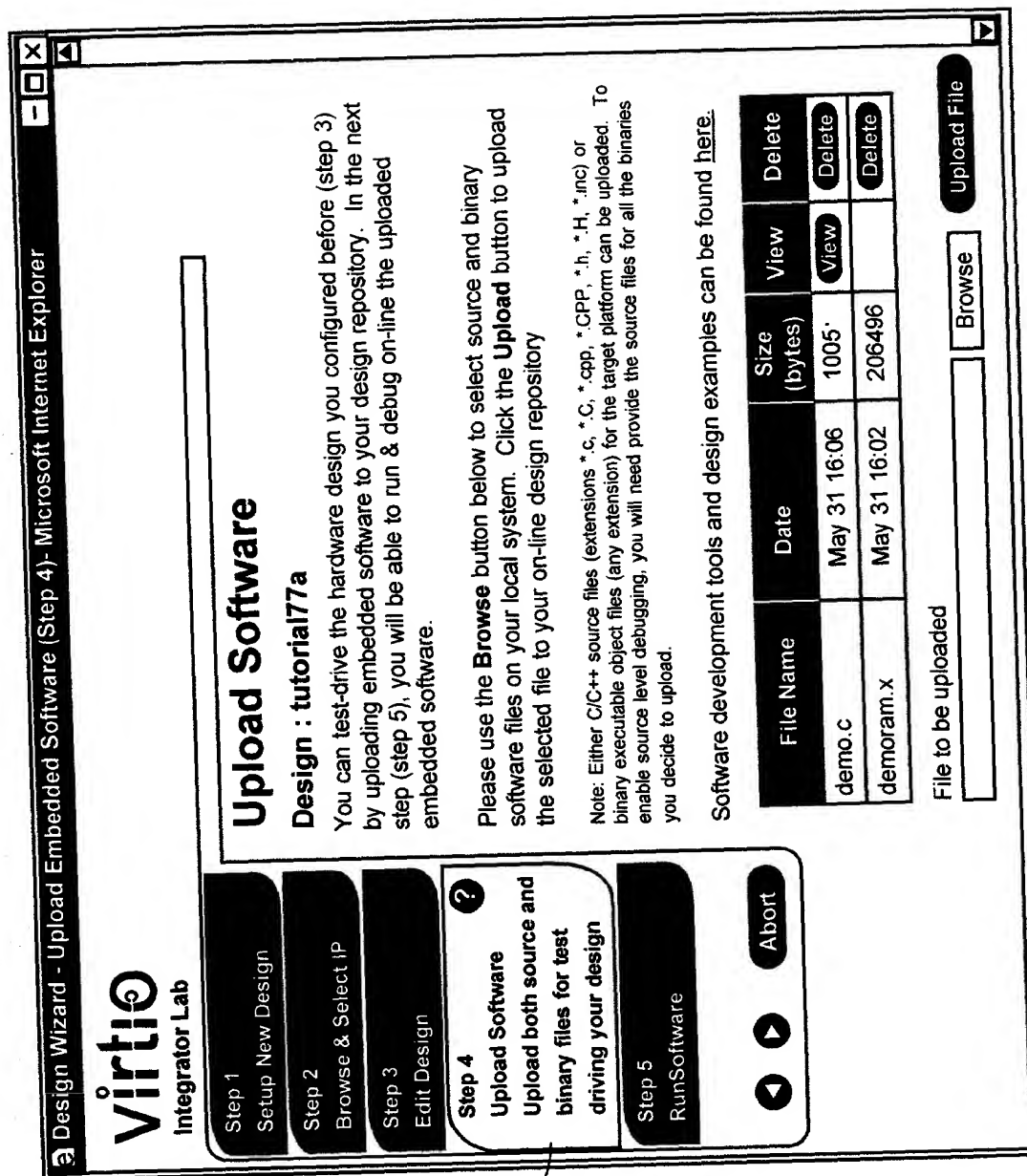


Fig. 54

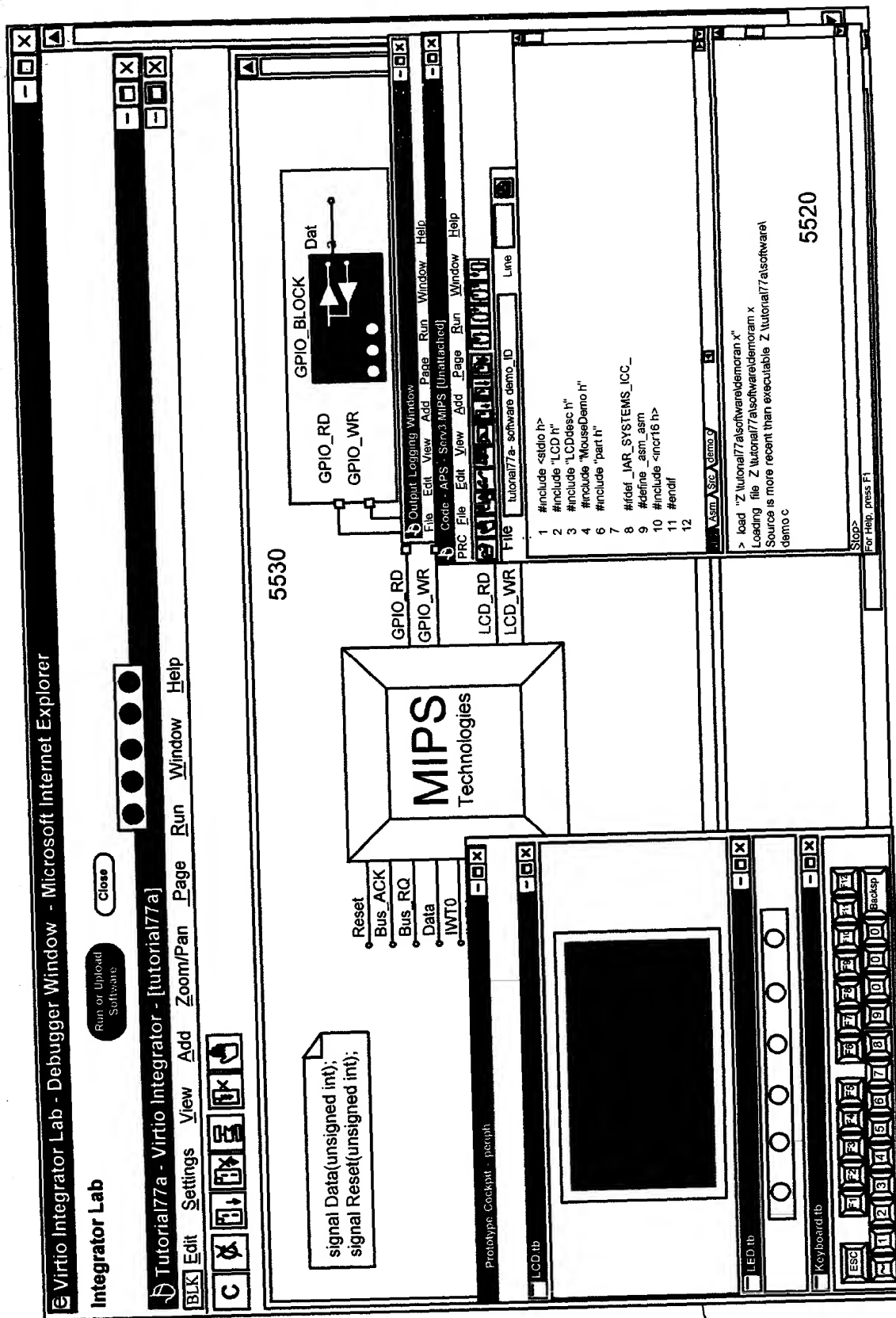


Fig. 55